2024 Q4 Cadence Taiwan Training Schedule

cadence

Click the 'Course Name' to see the course description

CourseCode	Course Name	Duration (Day)	Oct	Nov	Dec	Location	Fees /Per person (Tax Incl.)
Custom Design with Virtuoso Technology							
84460	Virtuoso Layout Suite L - IC6.1.8 //Virtuoso Layout Design Basics	1	15			Hsinchu	TWD 6,000
85081	Virtuoso Layout Suite XL -IC6.1.8 //Virtuoso Connectivity-Driven Layout Transition	1	30			Hsinchu	TWD 12,000
83018	Skill Language Programming -v6.1.8	2		21-22		Hsinchu	TWD 10,400
84453	Skill Programming for IC Layout Design - v6.1.6	1			20	Hsinchu	TWD 5,200
86253-6	ADE Explorer and Assembler v6.1.8 (S1~S4)	2		7-8		Hsinchu	TWD 12,000
84474	Virtuoso Spectre RF - v6.1	2	23-24			Hsinchu	TWD 12,000
82086	Analog Modeling with Verilog -A - Spectre17.1	1	29			Hsinchu	TWD 6,000
86241	Mixed Signal Simulations Using Spectre AMS Designer v20.09	1			3	Hsinchu	TWD 6,000
(Q2&Q4 only) 2024Q4	Physical Verification System (PVS) Training v22.1 - *Usage Introduction*	1			26	Hsinchu	TWD 12,000
86418	Quantus Transistor-Level v 19.1 - T1: Overview and Technology Setup; & T2: Parasitic Extraction	1	4			Hsinchu	TWD 6,000
Digital Design and Signoff							
86141	Innovus Implementation System (Block) v22.1	3			4-5-6	Hsinchu	TWD 18,000
86142	Innovus Implementation System (Hierarchical) v22.1	1			24	Hsinchu	TWD 6,000
82130	Abstract Generator - v5.1.41	1		1		Hsinchu	TWD 6,000
86143	Low-Power Flow with Innovus Implementation System v22.1	1	31			Hsinchu	TWD 6,000
86220	Genus Synthesis Solution with Stylus Common UI v22.1	2		19-20		Hsinchu	TWD 12,000
82169	Voltus Power-Grid Analysis and Signoff v22.1	2			12-13	Hsinchu	TWD 12,000
82147	Tempus Signoff Timing Analysis and Closure v22.1	1	22			Hsinchu	TWD 6,000
Equivalence Checking							
82123	Conformal Equivalence Checking v23.1	1	16			Hsinchu	TWD 6,000
82142	Encounter Conformal Constraint Designer (SDC/CDC Checks)	1		12		Hsinchu	TWD 6,000
82156	Conformal Low-Power Verification Using IEEE 1801 v22.1	1			19	Hsinchu	TWD 6,000
82194	Conformal ECO v23.1	1	3			Hsinchu	TWD 6,000
System Design and Verification							
86218	Xcelium Simulator v22.09	2		5-6		Hsinchu	TWD 12,000
86225	Xcelium Integrated Coverage V20.09	1		26		Hsinchu	TWD 6,000
82143	SystemVerilog Language for Verification v21.1	2			10-11	Hsinchu	TWD 10,400
PCB and Sigrity							
86263	Allegro Package Designer Plus v22.1	3		13-14-15		Hsinchu	TWD 18,000
(Q1&Q3 only) 2024Q3	Allegro High-Speed Constraint Management v22.1	2				Hsinchu	TWD 12,000
	Sigrity PowerDC and OptimizePI	2				Hsinchu	TWD 12,000
	PowerSI + Clarity : Wideband Model Extraction Technology	2				Hsinchu	TWD 12,000
(Q2&Q4 only) 2024Q4	XtractIM : Allegro Sigrity Package Assessment and Model Extraction	2	17-18			Hsinchu	TWD 12,000
	SystemSI – Basic	2		7-8		Hsinchu	TWD 12,000
	SystemSI – Advanced	2			17-18	Hsinchu	TWD 12,000

2024.9.3 updated

Remark ● **Cadence General Tool training= NTD 6,000** (per day/per person) ; **Cadence Language training: NTD 5,200** (per day/per person)