TECHNICAL **BRIEF**

cadence®

RF Through mmWave System Design with AWR Design Environment V22.1

Wireless technology, increasingly common in commercial products today, is driven primarily by the needs of emerging 5G/6G and internet of things (IoT) systems. The high-frequency semiconductor, PCB, and electronic packaging technologies initially developed to meet the needs of aerospace and defense applications are now being utilized to address the performance and reduced size, cost, and weight requirements of communications, industrial, scientific, medical (ISM), and automotive end markets. Traditionally, custom proprietary ICs, leveraging the latest advanced-node technology, set the standard for next-generation performance; however, the added demands of new RF- to millimeter-wave (mmWave)-enabled systems require an approach that moves beyond the chip.

This white paper highlights key features and functionalities in the V22.1 release of the Cadence® AWR Design Environment® platform that closes the gap between RF design and system integration, providing greater design support across IC, package, and board with new platform interoperability to enable front-to-back implementation and design verification workflows.

Design Overview

The call for greater functionality in a smaller footprint is being met with integrated heterogeneous technologies that include a complex mix of semiconductor devices combined with advanced interconnects and electronic packaging into next-generation products. System, IC, discrete component, laminate, package, and embedded antenna each have unique design and verification needs, leveraging the latest on- and off-chip manufacturing processes that drive performance and innovation. Therefore, multiple tools are required to deliver the breadth of analysis and design support needed to develop systems based on these different technologies. To expedite turnaround times, specialized high-frequency simulation and design optimization tools must include seamless, accurate modeling and multi-physics analysis, with the ability to share design data with the appropriate implementation platform for the target manufacturing process (Figure 1).

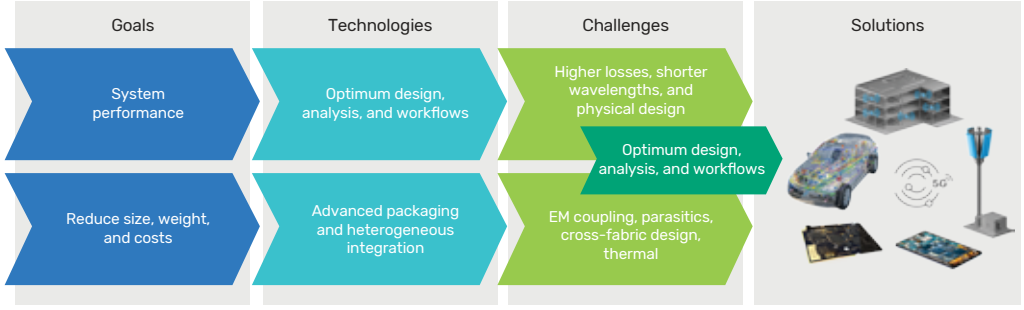


Figure 1. System, IC, discrete component, laminate, package, and embedded antenna each have unique design and verification needs

AWR Design Environment V22.1 accelerates the development of RF/microwave components and systems across monolithic microwave IC (MMIC), RFIC, package, module, and PCB technologies with design automation, enhanced RF simulation and device modeling, support for group design, accelerated optimization, powerful in-design analyses, and design for manufacturing workflows. Addressing in-design analyses requirements, the latest version of AWR® software offers enhanced integration of Cadence's Clarity™ 3D Solver and Celsius™ Thermal Solver to deliver unconstrained capacity for EM analysis of large-scale complex RF systems and electrothermal analysis of RF designs affected by power dissipation. Both solvers simulate using existing design data directly from within the AWR platform. The user doesn't need to switch tools, leave the simulation environment, or pass the design to a different engineering team for analysis (Figure 2).

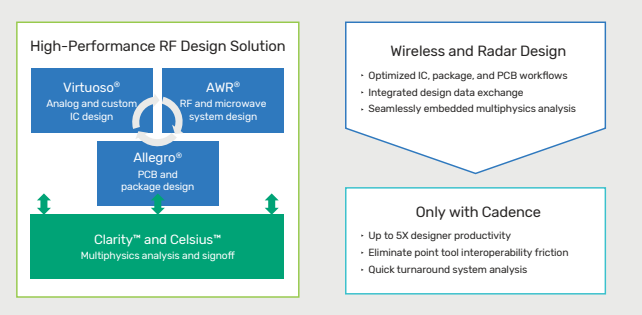


Figure 2: Cadence complete, interoperable system-level RF-aware design platform

The V22.1 release accelerates design data transfers between AWR Microwave Office® and the Cadence Allegro® System Capture front-end tool for schematic entry and high-level system architecture and Allegro PCB and Allegro Package Designer Plus layout editors for detailed board/package implementation. Furthermore, V22.1 introduces support for silicon-based MMIC design with direct reuse of Cadence Virtuoso process design kits (PDKs) and integration with the Cadence EMX® Planar 3D Solver, an electromagnetic (EM) simulator for high-frequency, RF, and mixed-signal silicon (Si) integrated circuits (Figure 3).

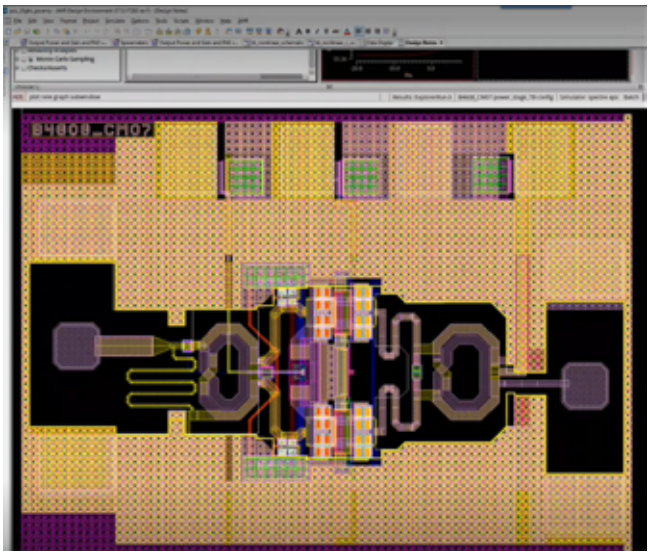


Figure 3: Si MMIC design for a 28GHz power amplifier (PA) using a Virtuoso PDK in Microwave Office software

The AWR Design Advantage

Accuracy

AWR software enables designers to capture true RF device and network performance with linear and nonlinear frequency-domain circuit simulation, extensive libraries of full-wave transmission line models, RF vendor components, gallium arsenide (GaAs) and gallium nitride (GaN) III-V foundry-authorized PDKs, and in-design EM analysis for electrically large structures, including full MMIC/package/PCB designs and thermal analysis for heat-generating RF power applications, directly within a single environment (Figure 4).

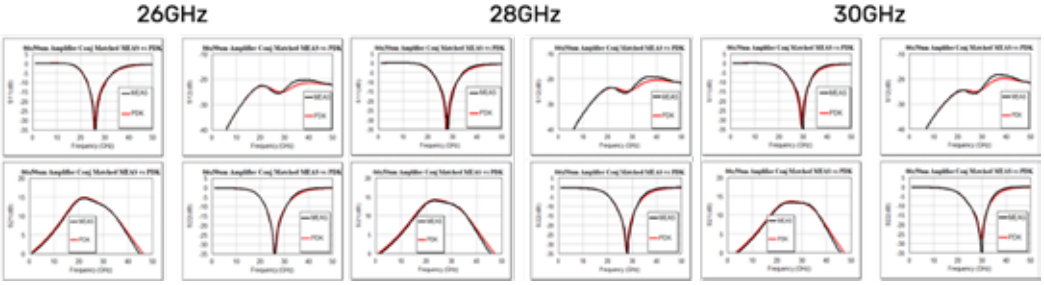
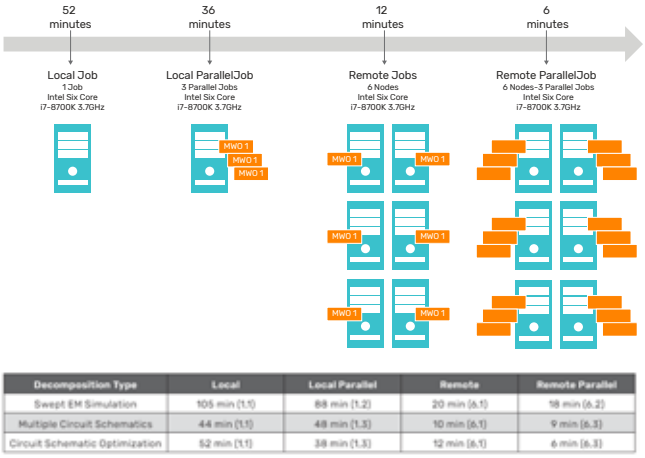


Figure 4: Microwave Office PDK results for 28GHz two-stage PA from UMS

Speed and Capacity

New design management capabilities, advanced layout and routing, version control for group-based product development, and improved synthesis and optimization enable engineering teams to accelerate their product development and reduce their overall turnaround time. Furthermore, with the increasing size of RF/microwave IP integration at both the IC and module packaging levels, it is often necessary to simulate RF networks with large, embedded S-parameters comprising up to thousands of input/output (I/O) ports over many frequency points, which results in lengthy simulation run times. Results for these big complex designs and/or parametric optimizations can be accelerated through AWR software support for remote and parallel circuit simulation. This gives designers access to more compute power to drastically cut EM and circuit-based simulation run times (Figure 5). As a result, design teams can perform more investigative studies and make more informed design decisions for a given period.



Decomposition Type	Local	Local Parallel	Remote	Remote Parallel
Swept EM Simulation	105 min (1.1)	88 min (1.2)	20 min (6.1)	18 min (6.2)
Multiple Circuit Schematics	44 min (1.1)	48 min (1.3)	10 min (6.1)	9 min (6.3)
Circuit Schematic Optimization	52 min (1.1)	38 min (1.3)	12 min (6.1)	6 min (6.3)

Figure 5: AWR V22.1 supports remote and parallel circuit simulation, providing access to more compute power

Accessibility

The AWR Design Environment platform provides accessibility and design support with added product functionality and more productivity-enhancing features, including improvements to the schematic and system editor, more Python scripting capabilities and support resources, improved Cadence Visual System Simulator™ (VSS™) system design software data file support, new RF measurements, expanded passive network synthesis, and new application-based tutorial design content. With RF IP created in AWR software, design teams can take advantage of Cadence enabled interoperable workflows for robust and efficient transfer of Microwave Office circuit design data to either the Allegro PCB design and/or Virtuoso RF Solution platforms for back-end design implementation and system integration (Figure 6).

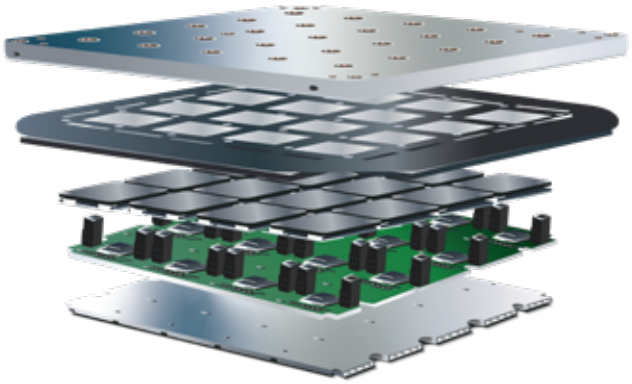


Figure 6: RF module created in the Virtuoso system design platform using integrated EMX, Clarity, Celsius, Microwave Office, and AXIEM analysis technologies

In-Design EM and Multiphysics RF System Analysis

As electronic devices integrate more functionality into shrinking footprints, the importance of EM and thermal analysis at the point of design, known as in-design, become critical to meeting aggressive delivery schedules and ensuring design success. As components designed in isolation are integrated into a package, module, PCB, or larger subsystem, unaccounted for EM and/or thermal behavior can often cause multiple design respins and product delivery delays. Designers need ready access to fast, accurate EM and thermal data throughout the entire physical design cycle to ensure that simulations accurately capture the behavior of the entire manufactured end-product. The solver integration technology built into the AWR Design Environment platform provides seamless accessibility to the Clarity 3D FEM and Celsius Thermal solvers for in-design analyses of RF systems with unprecedented speed, capacity, and accuracy.

Celsius Thermal Solver Integration

Designers can perform thermal analysis of power-dissipating MMICs, power amplifiers (PAs), temperature-sensitive RF filters, IC packages, RF PCBs, modules, and microwave/RF systems directly from within the AWR platform using the Celsius Thermal Solver. The structure, representing the IC, package, and/or board for thermal analysis, can be created by drawing or importing the geometry into AWR's EM editor or using the EM extraction block to automatically create a 3D thermal structure from an existing schematic/layout. Heat sources are easily defined as geometries drawn on a user-defined heat layer in a standard Microwave Office material stack-up or as an active device in a defined (scripted) parametric cell (PCell).

When a simulation is invoked, Celsius Thermal Solver performs thermal analysis using power dissipation data provided by a Microwave Office nonlinear (harmonic balance) circuit simulation without the need to exit the AWR environment. Operating temperatures for all heat-dissipating elements are reported in a table in the AWR software, and the latest release supports 3D thermal temperature distribution plots annotated directly onto the AWR 3D viewer for insight into hot spots and other areas of concern (Figure 7).

For RF designs that include electrothermal active devices, the resulting operating temperature from the Celsius simulation can be provided back to the device model, and RF nonlinear circuit simulation/thermal analysis is performed until the power versus operating temperature results converge. In addition, AWR software provides additional flexibility by enabling designers to launch the structure and save it in the Celsius Thermal analysis 3D environment directly from the AWR environment.

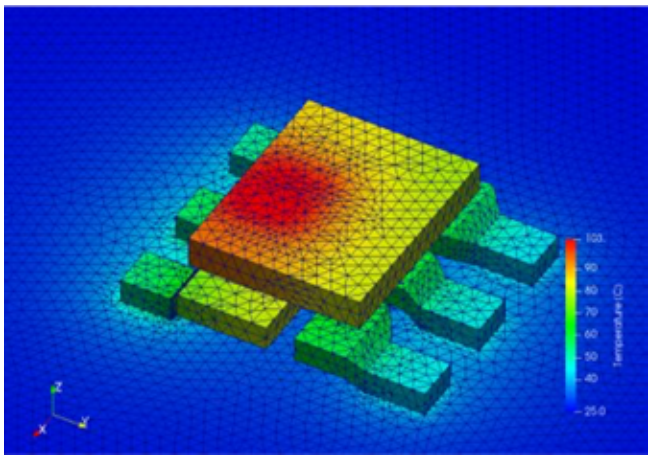


Figure 7: Celsius Thermal Solver performs thermal analysis using power dissipation data provided by Microwave Office software for added insight into hot spots and other areas of concern

Clarity 3D FEM Solver Integration

Using full-wave extraction for accurate S-parameter characterization of MMICs and modules containing multiple active devices such as field-effect transistors (FETs), high-electron-mobility transistors (HEMTs), and hetero-junction bipolar transistors (HBTs), can result in high-port count EM structures that require high-capacity solvers for timely results. The Cadence Clarity 3D FEM solver offers an industry-first solution for modeling these large RF structures initially developed for large signal integrity problems. The Clarity solver employs massive parallelization with initial mesh, adaptive mesh refinement (AMR), and adaptive frequency sweep (AFS) technology distributed across multiple servers to address larger 3D RF and high-speed problems faster without loss of 3D FEM accuracy (Figure 8).

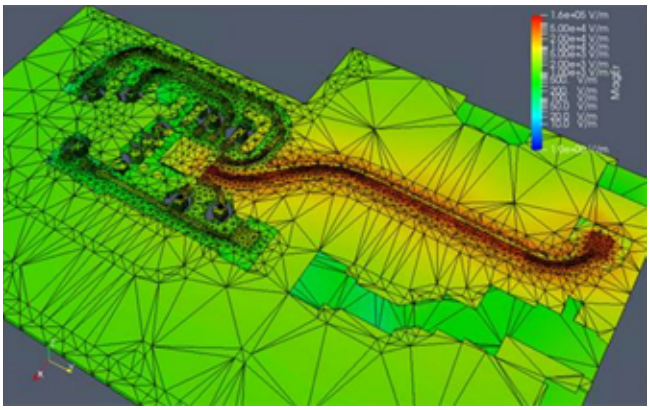


Figure 8: The Clarity solver employs massive parallelization with initial mesh, AMR, and AFS technology distributed across multiple servers to address larger 3D RF and high-speed structures

Ongoing developments in the Clarity 3D FEM solver for RF applications and enhancements to Clarity 3D integration in AWR software provide in-design 3D EM analysis of electrically large RF structures for co-simulation with Microwave Office software. Clarity 3D EM structures can be defined via user-controlled extraction from schematic/layout or as a structure created elsewhere using the AWR software's powerful PCB import feature or imported 3D CAD files. With any of these workflows, the Clarity solver uses distributed multiprocessing technology to deliver virtually unlimited capacity and 10X speed over legacy EM simulators. This enables engineers to address large RF designs such as entire MMICs in electronic packaging, cross-fabric modules, and die-on-laminate co-design.

RF Design Support

Synthesis

Beginning with the V22.1 release of AWR Design Environment, the component synthesis wizard and mixer and multiplier synthesis wizard are now available to all users with no additional licensing required. These innovative wizards enable faster design starts by generating commonly used RF functional blocks. The component synthesis wizard supports the synthesis of several types of passive microwave structures, including transformers, Wilkinson dividers, and various hybrid couplers (rat race, branch line, and Lange), implemented in microstrip transmission line structures (Figure 9).

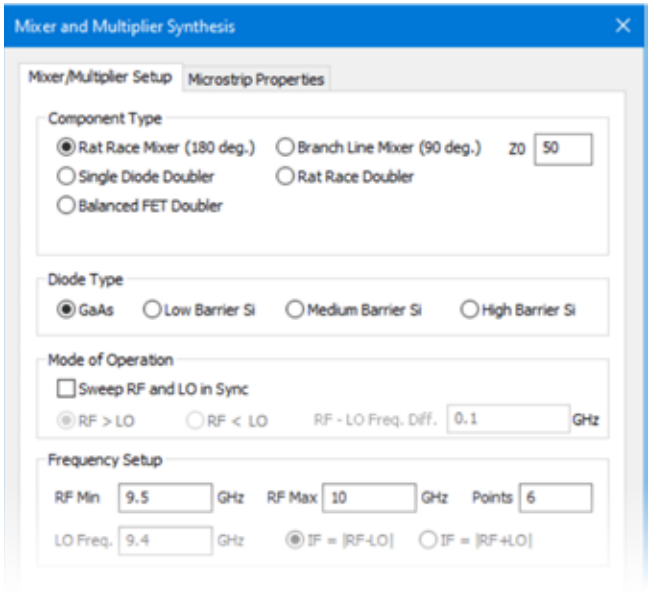


Figure 9: The component synthesis wizard and mixer and multiplier synthesis wizard enable faster design starts by generating commonly used RF functional blocks

The mixer and multiplier synthesis wizard enables the synthesis of several types of mixer and multiplier structures, also implemented in microstrip transmission line structures for easy integration with RF PCB subsystems. Hierarchical subcircuits and output graphs are created with each synthesized mixer, providing separate subcircuits for the hybrid combiner, diodes, and matching circuits and test circuits for simulating fixed and swept local oscillator (LO) power. Providing further support of RF mixer design and product development, AWR V22.1 also includes new design tutorials on setting up a harmonic balance simulation for mixer noise analysis and building a Microwave Office mixer subcircuit out of base components that generate LO harmonic mixer noise.

The component, mixer and multiplier synthesis wizards that are now included in the software complement the iFilter and network synthesis (impedance matching) wizards available as an add-on option.

New Hybrid Optimizer

AWR Design Environment software offers many optimization methods, all of which designers can select based on their experience with the quality of results or optimizer speed for a given problem type. Faster optimizers are often more sensitive to a problem's characteristics and parameters, while slower optimizers are frequently more robust. A new hybrid optimizer method has been added to AWR V22.1 offering a top-performance algorithm for an extensive range of optimization problems. As a result, the new pointer hybrid optimizer can achieve the user-specified optimization goal with fewer iterations, saving time while ensuring robust optimization. AWR optimization can be combined with the remote/parallel compute capabilities (add-on option) to accelerate simulation run times further and perform large-scale parametric design exploration (Figure 10).

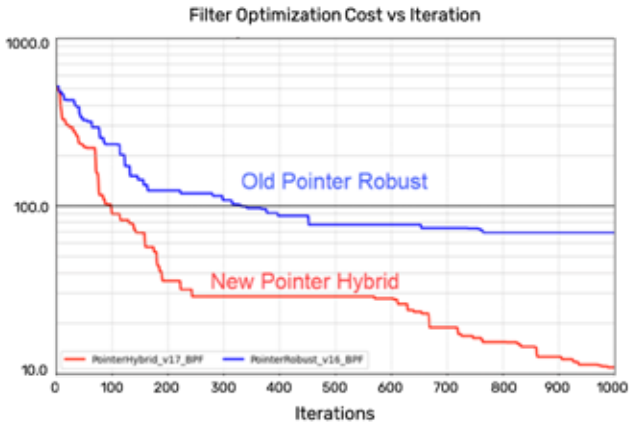


Figure 10: A new pointer hybrid optimizer in AWR software helps achieve the user-specified optimization goal with fewer iterations, saving time while ensuring robust optimization

Python Scripting Support

The AWR Design Environment platform has an extensive application programming interface (API) to facilitate custom scripting and design automation created by and for the end user. The API commands available with Visual Basic (VBA) can also be accessed using Python, providing access to a large body of readily available open-source libraries, including high-level math functions, digital signal processing, and highly flexible plotting functionality. The latest version of the software has added Python support resources, including a new getting started guide to assist users with Python scripting for design task automation and customization.

Version Control and Group Design

The AWR Design Environment platform supports the integration of version control software to effectively manage group design of complex, multi-function projects including integrated heterogenous technologies commonly found in multi-fabric RF modules. Version control supports collaboration between multiple designers, maintaining the revision history of design data in a central database or repository. The software manages and allows access to the file history and database of all files stored within (Figure 11).

For group design, version control software file management prevents unintentional file overwrites when multiple users edit the same file in the version control database or central repository. Version control, design rule checking (DRC), and subcircuit simulation caching for faster simulation run times of large networks are all available in the RF module design add-on option.

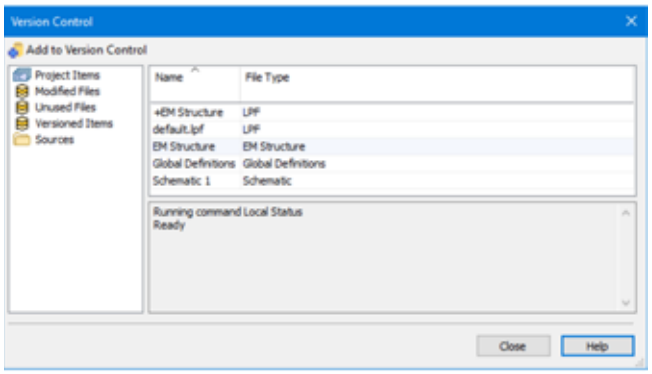


Figure 11: Version control manages and allows access to the file history and database of all files stored within

VSS Communications and Radar Systems Design

VSS communications and radar systems design software within the AWR Design Environment platform enables realistic measurements of mixed-signal (RF/digital) networks and cascaded RF blocks. It helps identify the source of spurious products and system metrics such as bit error rate (BER), all from a single system diagram, enabling designers of commercial and military transmitters and receivers to create subsystem architectures, specify component requirements, and optimize for best overall performance. Virtual 5G New Radio (NR) and IoT communication and radar/ electronic warfare (EW) systems can be conceptualized and rapidly implemented using RF/ microwave and signal processing blocks based on measured, simulated, or projected behavior to investigate new architectures and study overall system performance.

New data file utilities simplify the exporting/importing of waveform data for applications such as digital pre-distortion (DPD), device under test (DUT) evaluation, and communications receiver testing, supporting more efficient capture of waveforms from test hardware and other applications into VSS software. To facilitate signal demodulation in the tool, transmitter-generated signal properties blocks can save and reapply propagated properties from and to any signal in the software.

VSS testbenches can now apply standards-based communication signal generation and receiver functionality of Rhode & Schwarz test equipment to a virtual DUT (Figure 12).

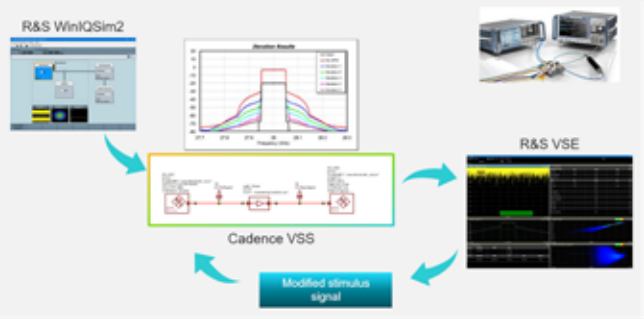


Figure 12: VSS testbenches can now apply standards-based communication signal generation and receiver functionality of Rhode & Schwarz test equipment to a virtual DUT

Standards-compliant signals can drive any VSS model, a Microwave Office subcircuit, or the VSS time delay neural network (TDNN) advanced amplifier behavioral model derived from Cadence Spectre® simulations. The joint solution linking Cadence and Rohde & Schwarz products provides VSS users access to fully vetted standard signals and measurements for analyzing their RF designs. It also ensures that the simulation excitation matches those used in the test lab for performance validation. They can use many pre-configured standard measurements and advanced offerings such as DPD algorithms. Furthermore, once the chips or RF links are built, the same setup can be replicated using hardware equipment with minimal effort in the lab.

Cadence Platform Interoperability

From automotive and industrial IoT applications to consumer products and medical equipment, virtually all intelligent systems today employ some form of communications and wireless sensing. Therefore, original equipment manufacturers (OEMs) developing intelligent systems need reliable workflows for RF IP development and integration across the chip, package, and PCBs. Platform interoperability being developed by Cadence provides the means to exchange design data efficiently across dedicated implementation tools.

Since all RF performance is directly linked to any design's physical attributes, circuits developed in Microwave Office software require information about the manufacturing process, which includes the material stackup and drawing layers. The material stackup, whether a semiconductor such as GaN or a substrate such as alumina or FR4, is specified in a substrate definition block used by the distributed transmission line models for RF simulation. For MMICs, the foundry usually provides the stackup information in the form of a PDK, including simulation models, IC component layout PCells, and DRCs. For PCBs, this stackup information is determined by the manufactured board technology as agreed upon by the various design teams responsible for the overall system.

To successfully integrate the RF IP created in Microwave Office software into the Allegro PCB Design Editor, the component libraries (symbols and footprints) and process technology data must be coordinated across the two platforms to ensure the design data compatibility. Often this integration is performed manually by a layout engineer with limited knowledge of RF circuit behavior relying on input from the RF team, resulting in time-consuming and costly design re-entry and the potential for design failure. Platform interoperability avoids these challenges by aligning the data used in each respective environment and automating design data transfer more efficiently to ensure design integrity.

The V22.1 release of AWR software provides enhanced cross-platform interoperability supporting the reliable transfer of RF schematic and layout IP from Microwave Office software to the Virtuoso and/or Allegro platforms for system integration, signoff, and manufacturing. This enables engineering teams to design, verify and pass their completed RF IP to either the Allegro PCB and system-in-package (SiP) or Virtuoso platforms for physical implementation using Cadence tools as the primary PCB, package, or IC implementation platform, with AWR software providing the RF IP schematic/layout design data.

RF-to-PCB Manufacturing Workflow

Platform interoperability enhancements in AWR V22.1 allow layout engineers using the Allegro platform to integrate RF design data from AWR software (Figure 13).

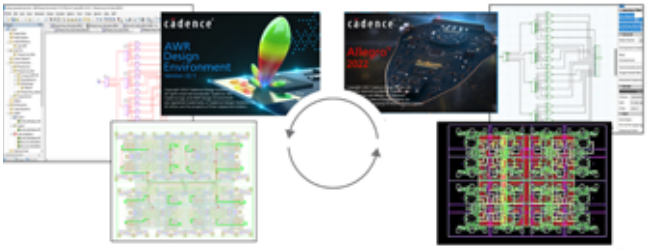


Figure 13: Platform interoperability enhancements in AWR V22.1 allow layout engineers using the Allegro platform to integrate RF design data from AWR software

This eliminates manual design reentry and ensures the design data is identical to the version developed by the RF engineering team by aligning the data to both the RF design and its defining components and the data used in the layout environment. Design data includes drawing and material layers, which define metal layers used for RF traces and can be characterized through EM analysis in the AWR platform, as well as surface-mount components and the physical footprint and padstack definitions. When the RF design is complete, the engineer can easily export the design as a new Cadence unified design library, which packages all the information for the layout engineer to integrate the RF design into their PCB design.

MMIC and Module Design

High-performance, cost-sensitive silicon (Si) products in sophisticated wireless devices are often implemented in highly integrated, multidevice, and multi-fabric modules. While device geometries have shrunk from hundreds of nanometers to a few nanometers, allowing ICs produced at smaller technology nodes to offer dramatically improved performance, complementary metal-oxide semiconductors (CMOS) alone cannot meet the requirements necessary in the high-frequency space. Therefore, technologies better suited for RF to millimeter-wave applications, including MMICs developed in Silicon germanium (SiGe), GaAs, GaN, and indium phosphide (InP), along with filter technologies, such as surface acoustic wave (SAW) and bulk acoustic wave (BAW), are combined with advanced-node Si at the module or packaging level using a host of techniques.

Advanced package/module interconnect technologies can include micro bumps, stacked die, interposers, fan-out, and multi-layer substrates, resulting in complex design stackups and data sourced from various design teams using different design platforms. If the interconnects carry RF signals, they

must be designed for optimal RF integrity with the appropriate EM and thermal analysis technologies.

RF design may also be called for if distributed passive components such as couplers, filters, or antennas are embedded directly into the module. For successful module integration, design data from one analysis platform must be accurately captured in the platform responsible for manufacturing. In Cadence tools, MMIC and off-silicon RF design data, including schematics and layout developed in AWR software, can be exchanged with the manufacturing layout tool responsible for managing the multi-technology integration.

AWR/Virtuoso Interoperability and PDK Reuse

The Cadence Virtuoso Analog Design Environment (ADE), Cadence Spectre® Simulation Platform, and the Spectre RF Option address this integration challenge with the most widely used platform in the electronics design industry. The Virtuoso custom IC design platform offers advanced multi-technology, schematic-driven, hierarchical design capabilities and is supported by more foundries than any other EDA tool.

The AWR Design Environment platform now includes an RF/microwave design creation environment with an export pathway to the Virtuoso Schematic Editor and Virtuoso Layout Suite. Designers can now create and analyze Si RF/mmWave IP utilizing Virtuoso PDKs in Microwave Office software and share the schematic and layout with Virtuoso software ready for analysis, design integration, and backend verification flows. Interoperability between these software tools facilitates the design and analysis of RF/microwave, analog, and digital design elements.

EMX 3D Planar Solver Integration

EM analysis on Si Virtuoso PDK RF circuit designs can be run from within the AWR platform using the Cadence EMX Planar 3D Solver (Figure 14). The EMX solver is an EM simulator optimized for high-frequency, RF, and mixed-signal Si ICs. It allows designers to accurately and efficiently simulate large RF circuit blocks, characterize the behavior of passive components, and analyze the parasitics due to interconnect. The EMX Planar 3D Solver's unique emphasis is on complete automation with uncompromised speed and accuracy. The tool has been benchmarked to be more than an order of magnitude faster than the industry's leading finite-element and boundary element tools.

Virtuoso PDKs, including those enabled for Microwave Office, offer EMX-based PCells to automatically generate a layout for on-chip passive components as defined by a particular foundry tech file and design for manufacturing (DFM) tech files, so they are design rule clean by construction. The EMX solver is extremely efficient and accurate at solving Si IC structures and is widely supported by foundries. New Virtuoso PDKs enabled for Microwave Office software can include foundry-approved EMX passive components.

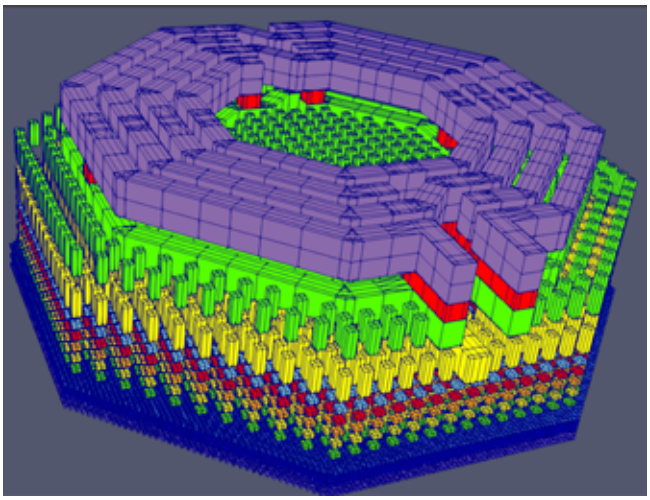


Figure 14: EM analysis on Si Virtuoso PDK RF circuit designs can be run from within the AWR platform using the Cadence EMX Planar 3D Solver

Enhanced Spectre RF Integration and Spectre Netlist Import Utility

For cases where the RF design focus is within the module fabric but requires an electrical representation of the Si IC itself, Microwave Office software now supports the easy setup of Spectre RF simulation in the AWR Design Environment platform with a new Spectre tab within the circuit options dialog box for embedded Spectre netlists in an AWR project. A new utility script allows users to import Spectre netlist blocks, creating schematic symbols that can be simulated with a VSS testbench or embedded into an AWR project (network) for RFIC/module co-design. This allows the RF design team focusing on the module to incorporate critical parts of the RFIC into their simulations, as might be the case for off-chip tuning, impedance matching, etc.

Conclusion

Next-generation RF- to-mmWave-enabled systems for emerging 5G/6G and IoT systems require an approach that provides greater design support across the entire IC, package, and board, with platform interoperability that enables front-to-back implementation and design verification workflows. This white paper has discussed features in AWR 22.1 software that closes the gap between RF design and system integration by addressing in-design analysis requirements through enhanced integration with the Clarity 3D Solver and Celsius Thermal Solver. Accelerated data transfers with Allegro tools for detailed board/package implementation have been highlighted, as well as the reuse of Virtuoso PDKs and integration with the EMX Planar 3D Solver for high-frequency, RF, and mixed-signal Si IC simulation.

AWR Design Environment V22.1 accelerates the development of RF/microwave components and systems across MMIC, RFIC, package, module, and PCB technologies with design automation, enhanced RF simulation and device modeling, support for group design, accelerated optimization, powerful in-design analyses, and design for manufacturing workflows.

cadence®

Cadence is a pivotal leader in electronic systems design and computational expertise, using its Intelligent System Design strategy to turn design concepts into reality. Cadence customers are the world's most creative and innovative companies, delivering extraordinary electronic products from chips to boards to complete systems for the most dynamic applications. **www.cadence.com**