SUCCESS **STORY**

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Qorvo and Cadence

GaN Discrete PA Design Using AWR Software

Key Challenges

To create this hybrid discrete power amplifier (PA), Qorvo wanted to provide a highly broadband solution that was inexpensive and had a small footprint, but this made implementing multiple stages a difficult task given size constraints. The designer chose to use a bridged T topology because it allowed him to match the input of a single transistor to 50Ω while minimizing die area. The packaged amplifier needed to demonstrate 5W of output power and 40-50% power-added efficiency (PAE) across the 1 – 2.7GHz range.

The transistor was sized such that the 50Ω termination on the output matches well to its target load line, so that the output can be left unmatched. A transistor with 1.24mm periphery was chosen, and, additionally, a transistor with 2.48mm periphery was also designed, which provides a favorable load line and similar die area, but was not used in this design. The final monolithic microwave integrated circuit (MMIC) used for the hybrid discrete PA solution is shown in Figure 1.

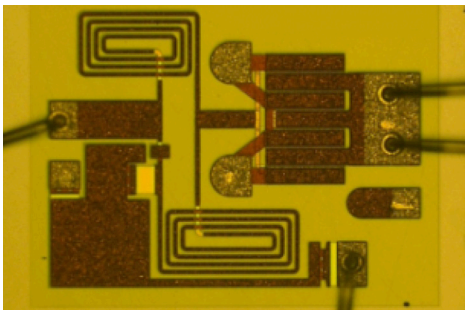

Figure 1: Fabricated MMIC used for the hybrid discrete PA solution

Application

- Qorvo Hybrid Discrete Power Amplifier

Software

- Cadence® AWR Design Environment® Software Portfolio, including:
  - Cadence AWR® Microwave Office® Circuit Design Software
  - Cadence AWR AXIEM® Planar Electromagnetic (EM) Simulator

Benefits

- Ease of use
- User productivity
- Reduction in design time

Solution

Cadence AWR Microwave Office circuit design software was used for the linear simulations, which were matched to imported S-parameter blocks. The Cadence AWR AXIEM 3D planar electromagnetic (EM) analysis was used for the board-level layout and EM simulation of the input and output matches.

The designer was more easily able to design the matching networks thanks to the built-in tools and measurements within the Cadence AWR Design Environment® platform.

The software's ability to easily construct, compare, and optimize various topologies quickly was another advantage. The highly integrated AWR AXIEM tool was especially helpful with the extraction flow for the board design.

The final device was tested on a board made of Rogers 4350B. The 50Ω-matched input held up well enough to achieve 10dB return loss from 40MHz to 2.7GHz and 7dB return loss down to 30MHz, as shown in Figure 2. The device achieved a gain of 12dB at lower frequencies and 17dB at higher frequencies.

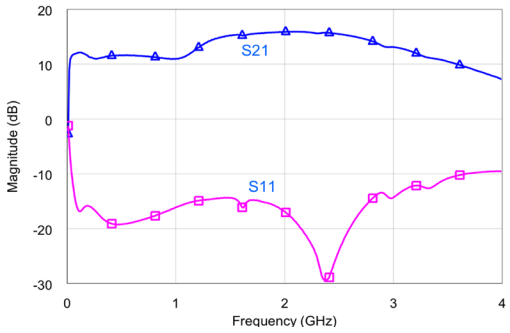

Figure 2: Small signal S-parameters for a hybrid MMIC discrete PA.

At 32V and under pulsed conditions, the amplifier achieved a typical output power of 5W (or 4W/mm power density) and 45% PAE over 1 to 2.7GHz, as shown in Figure 3.

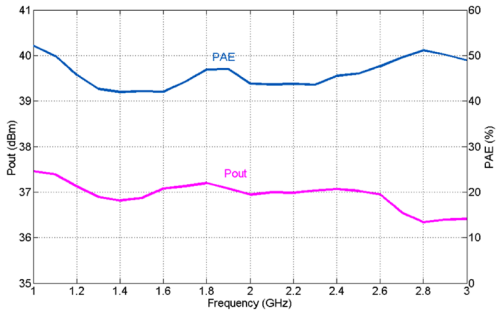

Figure 3: Measured P_{out} and drain efficiency of the hybrid solution, where the amplifier was driven to 3dB compression and used a 100us pulse width with 20% duty cycle

The pulsed operation was chosen over continuous wave (CW), because the evaluation board limited the total power dissipation. Additionally, the data were measured from 1 to 2.7GHz, because the designer was not able to set up a pulsed test station below 1GHz.

The engineer reused the design for several MMICs of different power levels with the bridge T input match. The product using the 2.48mm is complete and shows excellent results.

Summary

The designer chose AWR software because, having used it as an engineering student, he now prefers it to other RF design tools, especially its ease of use. He noted that the unified database with tightly integrated schematic and layout is especially beneficial because it makes it much easier to understand projects and what is actually being designed, modeled, and laid out.

> *Being able to lay out everything in the Cadence AWR software quickly and correctly and to send it straight to be manufactured has allowed me to complete design cycles in a short time.*
>
> Mark Greene, Qorvo

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