

Baseband IC Design Kits for Rapid System Realization

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cadence[®]

Agenda

How to Speed Up IC Volume Production

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Cadence Design Systems
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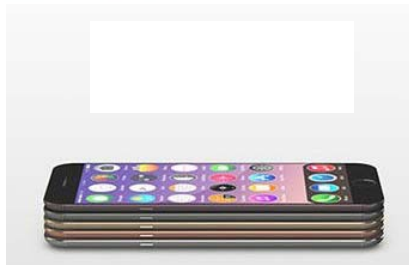
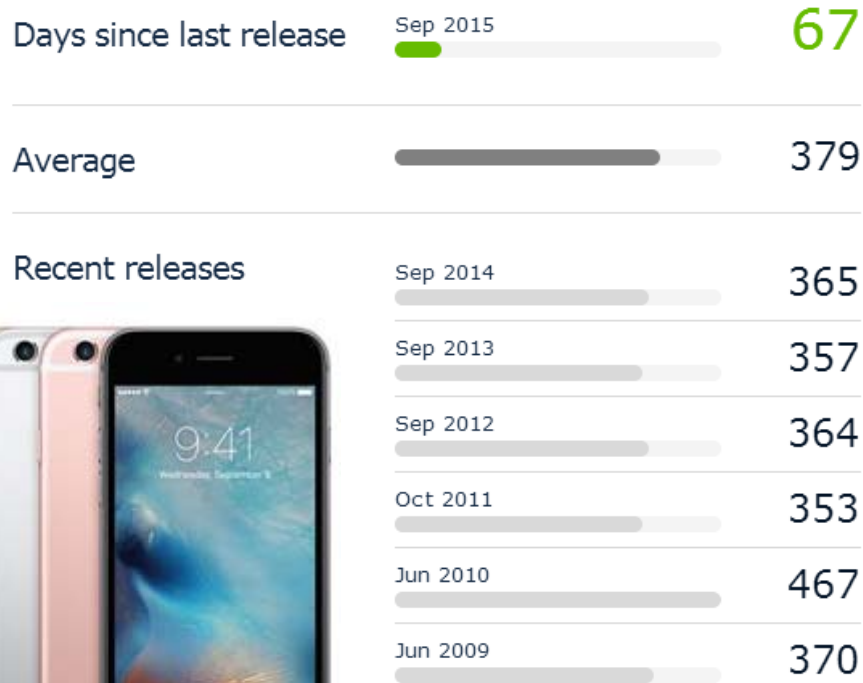


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Life of Electronic Device Getting Shorter



Jul 2016

Competition - Market Share



Jan 2016



Jan 2016



Sep 2015

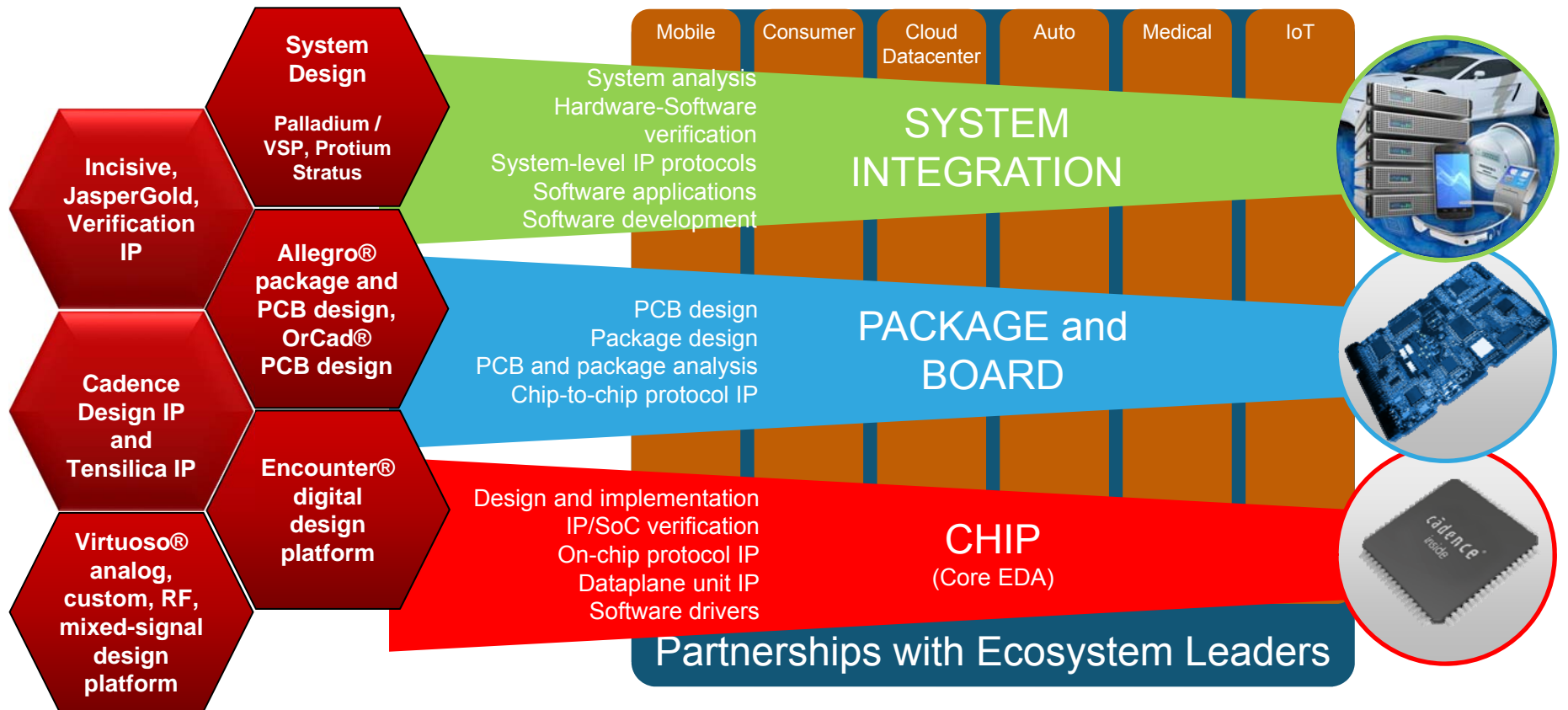


Apr 2015

Life Cycle

Cadence System Design Enablement

From end product to chip



Roadmap to Best-in-Class Product Creation

Attributes and practices from a survey of 500+ leading systems companies

Allegro advanced fabrication support (HDI, embedded, rigid / flex etc.)

ECAD / MCAD

Component selection across multiple databases

Thermally aware signal and power integrity

Centralized component library

Allegro Library Workbench

Sigrity

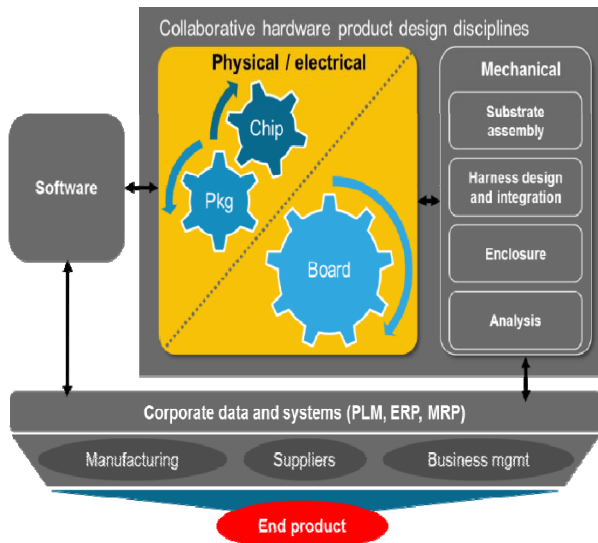
Allegro Design Workbench

Allegro PCB with all major MCAD tools

Allegro PCB

Allegro Sigrity Integrated Solution

Better together – makes product creation predictable

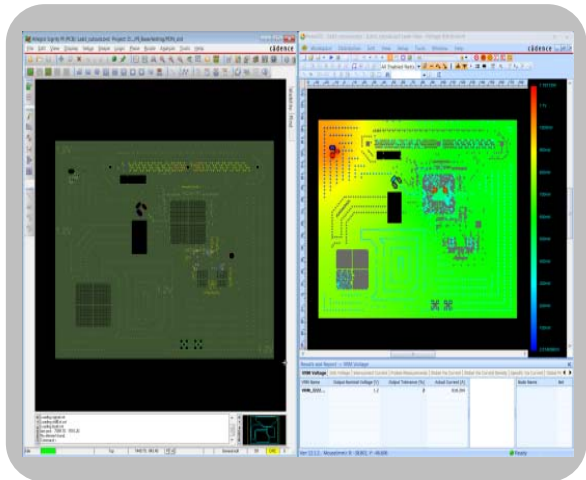


Allegro® constraint-driven PCB design flow endorsed by customers since 2001

- Predictable design cycles
- Accelerate time-to-volume production
 - Eliminate unnecessary design iterations
 - Route and tune standards-based interfaces 4X faster
- Early prototyping with Sigrity™ technology from Allegro platform creates robust reusable PCB constraint IP

Sigrity tool's unique power-aware SI/PI analysis and signoff ensures designs work right the first time

- Accelerate time-to-volume production
 - Validate multi-gigabit interfaces are compliant
 - Eliminate prototype iterations
- Reduce end-product cost by optimizing decoupling capacitors
- Integrated with Allegro PCB and IC packaging design solutions

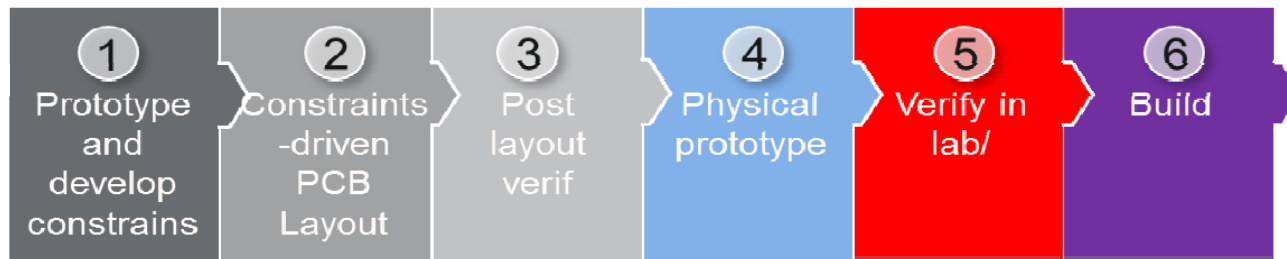


Integrated design and power analysis

Shorter, Predictable Design Cycles with Allegro Constraint-Driven Design Flow



Traditional PCB and EDA design flow supports a subset of constraints



Allegro constraint-driven PCB design flow

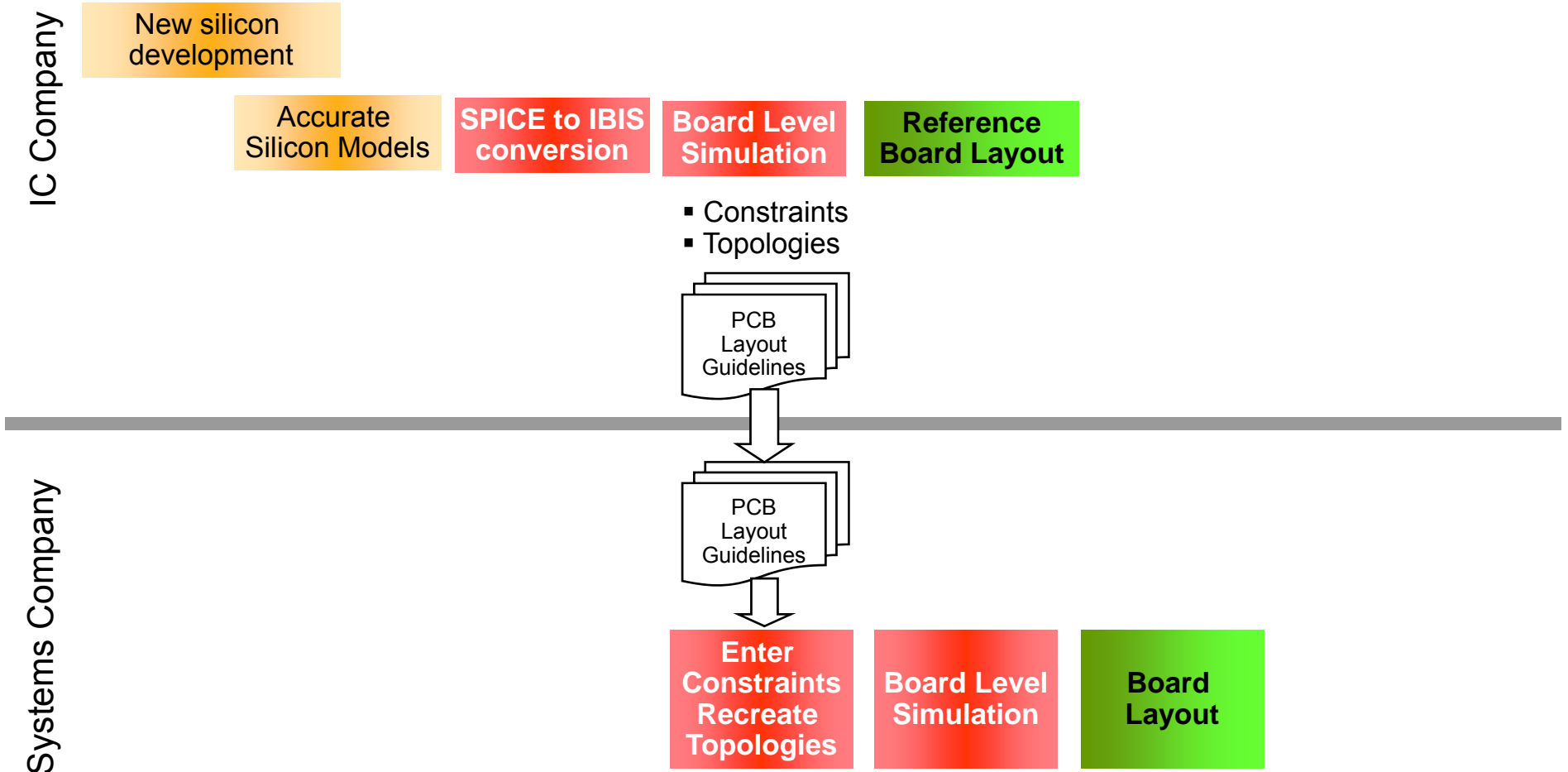
Up to 30%

Significant reduction in design cycles reported by customers

Major boost in PCB design productivity

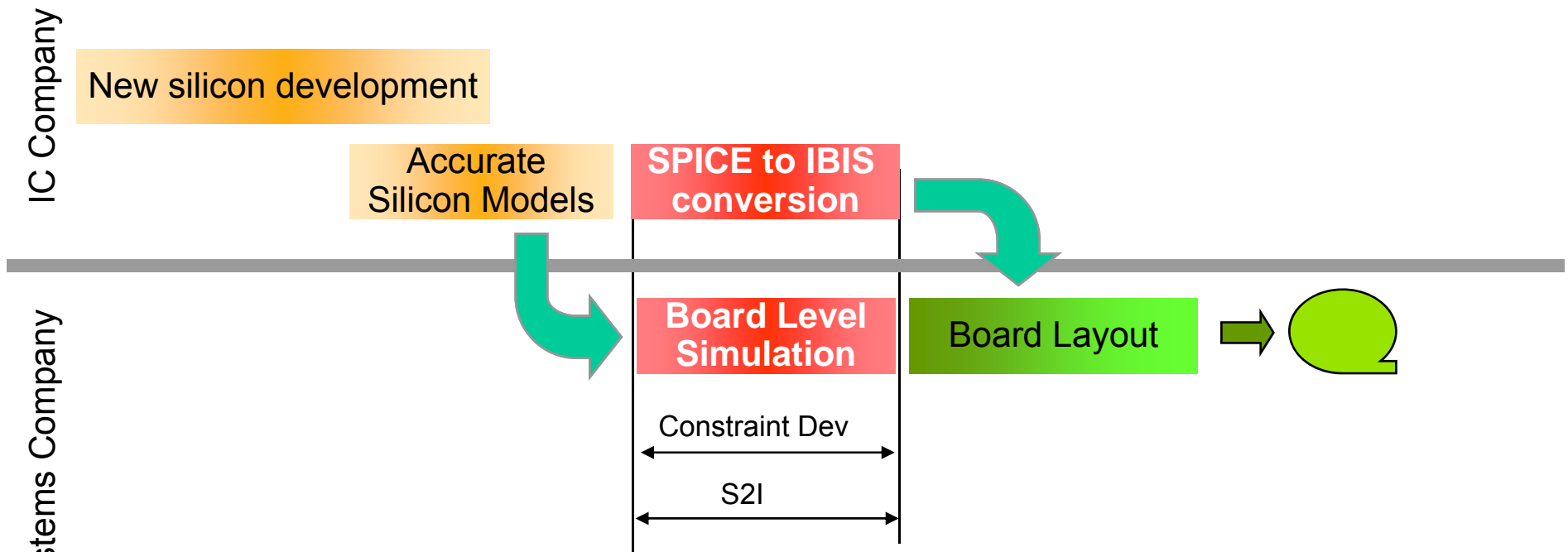
Unmatched breadth and depth of constraints to tackle any design

Duplicated Effort for IC and System Design in Current Design Flow



High Efficient Design Flow Driven by Cadence Methodology

- Shorten your customers time to implement new devices / architectures on PCB systems



- Provide design kits in electronic plug-n-play form enabling customers to design-in new devices/architectures in shortest amount of time possible

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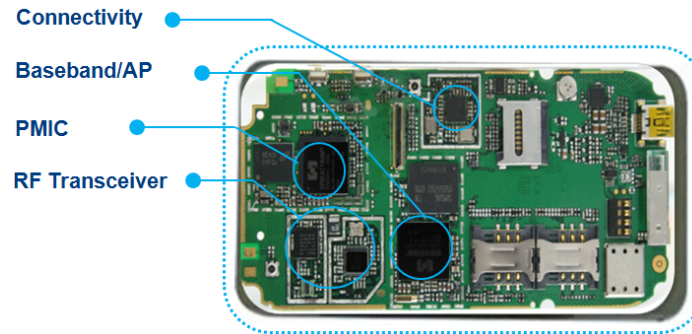
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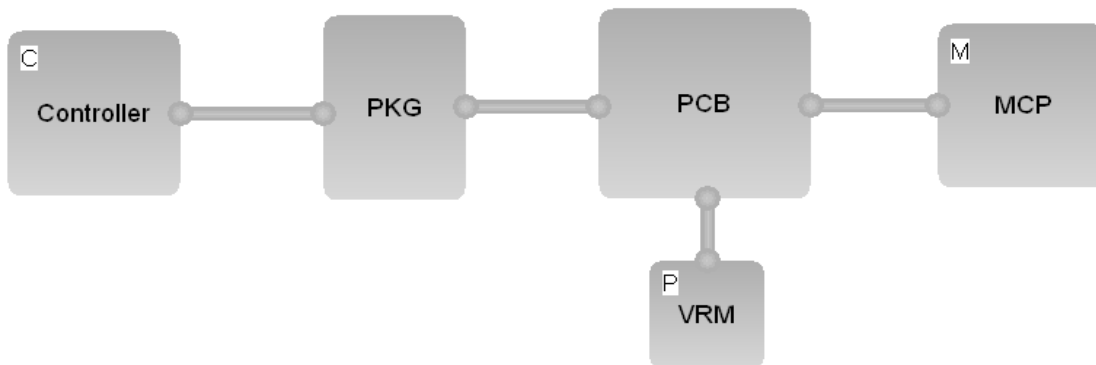
What's in a Design-in kit

- A design-in kit is a **Virtual Reference Design (VRD)**

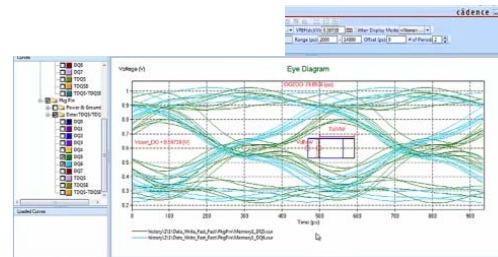
– All the stuff here:



– Is modeled here:

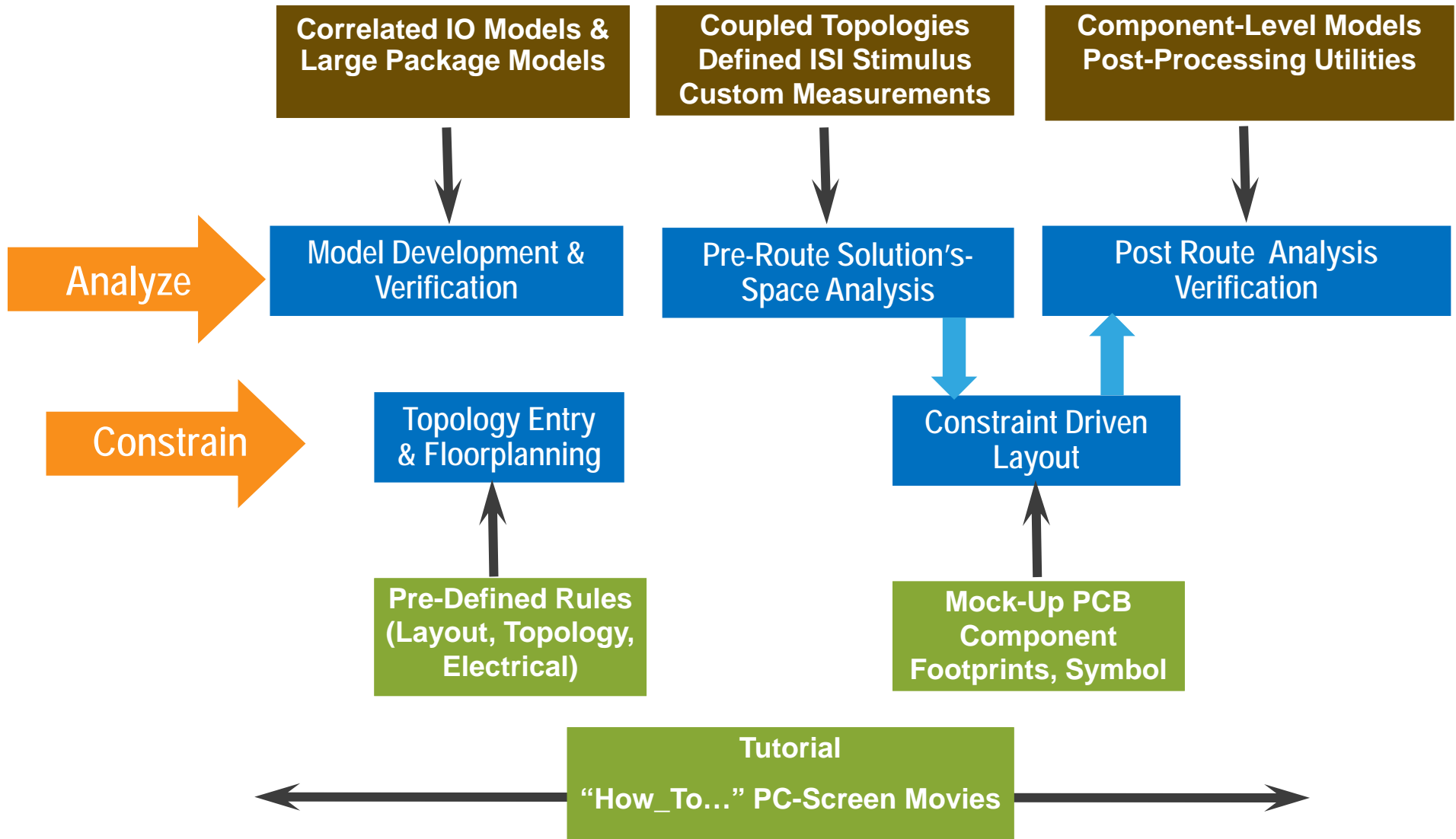


Measurement results are replaced with simulation results



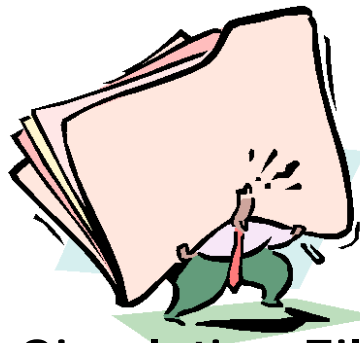
Sigrity System SI

Design-in kit & Development Cycle

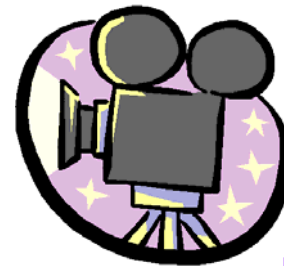
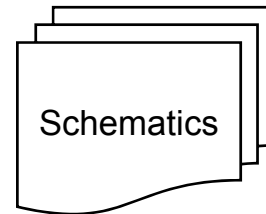


Design-in kit Contents

- A collection of design and simulation plug-n-play modules, scripts and utilities for Cadence Allegro/Sigrity tools that shorten the time to design-in new IC devices/platforms

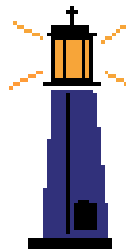


Simulation Files
Models, Topologies, etc.

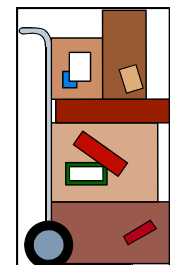
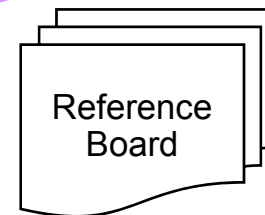


Tutorial Movies

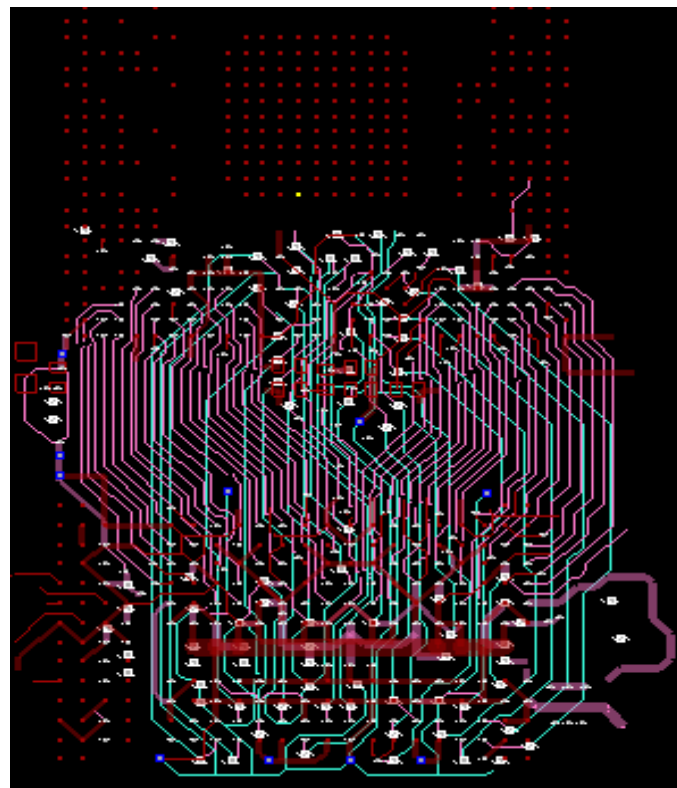
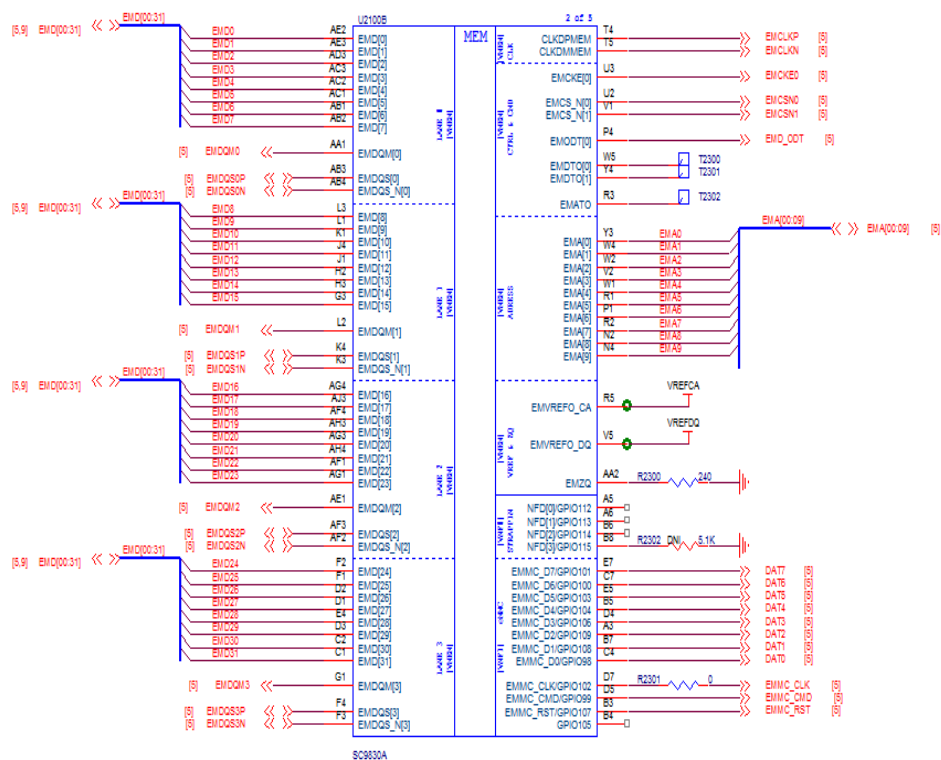
...all organized into a web-site



Automated
Layout Guideline
Constraint Files



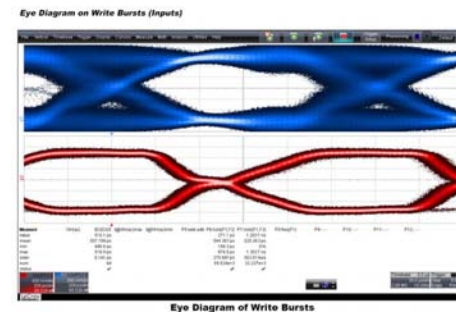
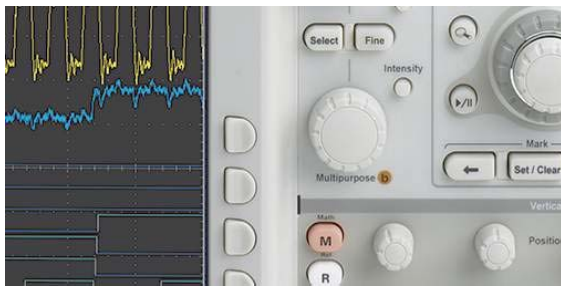
Board Level Reuse in Design-in kit



LPDDR (2)	LPDDR	0.0750:0.0750...	0.0000	0.2032	0.0000					0.0000	0.0750:0.1250...	0.0000	0.0000	0.0000
ADD_CTRL_CLK (2)	LPDDR	0.0750:0.0750...	0.0000	0.2032	0.0000					0.0000	0.0750:0.1250...	0.0000	0.0000	0.0000
ADDRESS (10)	LPDDR	0.0750:0.0750...	0.0000	0.2032	0.0000					0.0000	0.0750:0.1250...	0.0000	0.0000	0.0000
CTRL_CLK (5)	LPDDR	0.0750:0.0750...	0.0000	0.2032	0.0000					0.0000	0.0750:0.1250...	0.0000	0.0000	0.0000
DATA (4)	LPDDR	0.0750:0.0750...	0.0000	0.2032	0.0000					0.0000	0.0750:0.1250...	0.0000	0.0000	0.0000
LANE0 (10)	LPDDR	0.0750:0.0750...	0.0000	0.2032	0.0000					0.0000	0.0750:0.1250...	0.0000	0.0000	0.0000
LANE1 (10)	LPDDR	0.0750:0.0750...	0.0000	0.2032	0.0000					0.0000	0.0750:0.1250...	0.0000	0.0000	0.0000
LANE2 (10)	LPDDR	0.0750:0.0750...	0.0000	0.2032	0.0000					0.0000	0.0750:0.1250...	0.0000	0.0000	0.0000
LANE3 (10)	LPDDR	0.0750:0.0750...	0.0000	0.2032	0.0000					0.0000	0.0750:0.1250...	0.0000	0.0000	0.0000

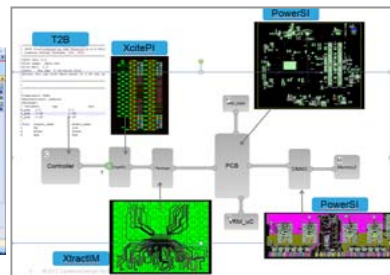
Signal & Power Integrity Simulation Reuse with Measurement Correlation Data

- Tested and verified in the lab and compared to Sigrity simulation
 - Results are correlated with test and measurement equipment
- It starts with silicon correlated I/O (IBIS) models
- Interconnect extracted with industry leading field solvers from Sigrity model signal, power, and ground coupled together.

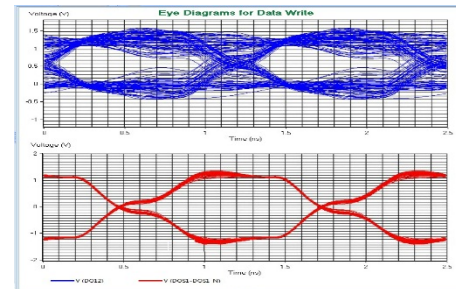


PCB

Package



System Simulation



Correlated Results



DesignKit Helps Win-Win by Designing For Your Customer

- Make new devices/architectures easy to design-in

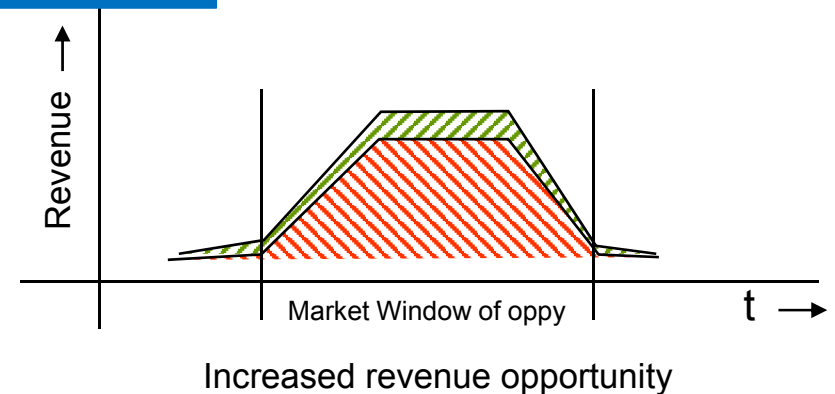
- Fast Time to Market

- Larger market share
- Higher revenues
- faster return on investment

- High quality design with proven data

- Differentiated and Improved customer support makes for a preferred vendor

- Instant productivity
- Reliable & proven data
- Shorter design cycle



Cadence and Spreadtrum Collaborate on Virtual Reference Design Kit to Reduce Customers' Design Cycle by Up to 12 Weeks

- Cadence® Allegro® PCB Designer (layout and schematic)
- Cadence Sigrity™ PowerDC™ (DC Power Integrity) technology
- Cadence Sigrity Power SI® (AC Power Integrity) technology
- Cadence Sigrity power-aware SI flow for LPDDR

Design and Spreadtrum announced they have developed a virtual reference design kit specific to Spreadtrum's [SC9830A](#) quad-core system-on-chip (SoC) platform requirements.

The availability of the kit enables joint customers to accelerate their mobile product and application design cycles by **up to 12 weeks**, including time spent on schematic design, PCB design and power-aware signal integrity (SI) and power integrity (PI) signoff simulation.



“We worked very closely with Cadence, leveraging their Sigrity technology, to develop a virtual reference design kit that makes it easier for our customers to design in our SC9830A quad-core SoC,” said John Rowland, SVP of Hardware Engineering at Spreadtrum. “Our customers can now begin to optimize the cost and performance of their products to take advantage of all the Spreadtrum SC9830A features, while meeting accelerated time-to-market challenges.”

Design-in kit Folder Structure

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Thank You

