

# Panel Session TP-TU3 High-speed Channel Designs IBIS AMI Solution

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Designcon 2009  
February 3, 2009

# Challenges

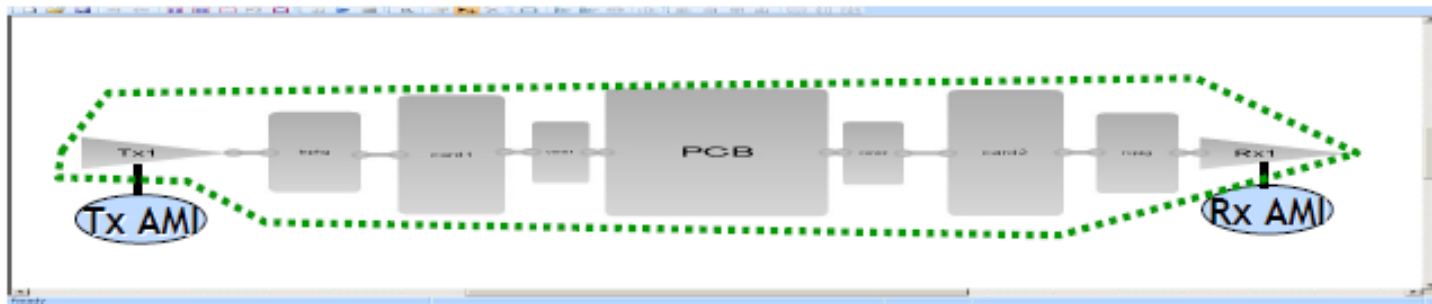
- Modeling of Equalization schemes including FFE, DFE
- Representing Clock and Data Recovery
- Computing Bit Error Rates == High Simulation Performance
- Architectural Exploration

# Algorithm Level Modeling

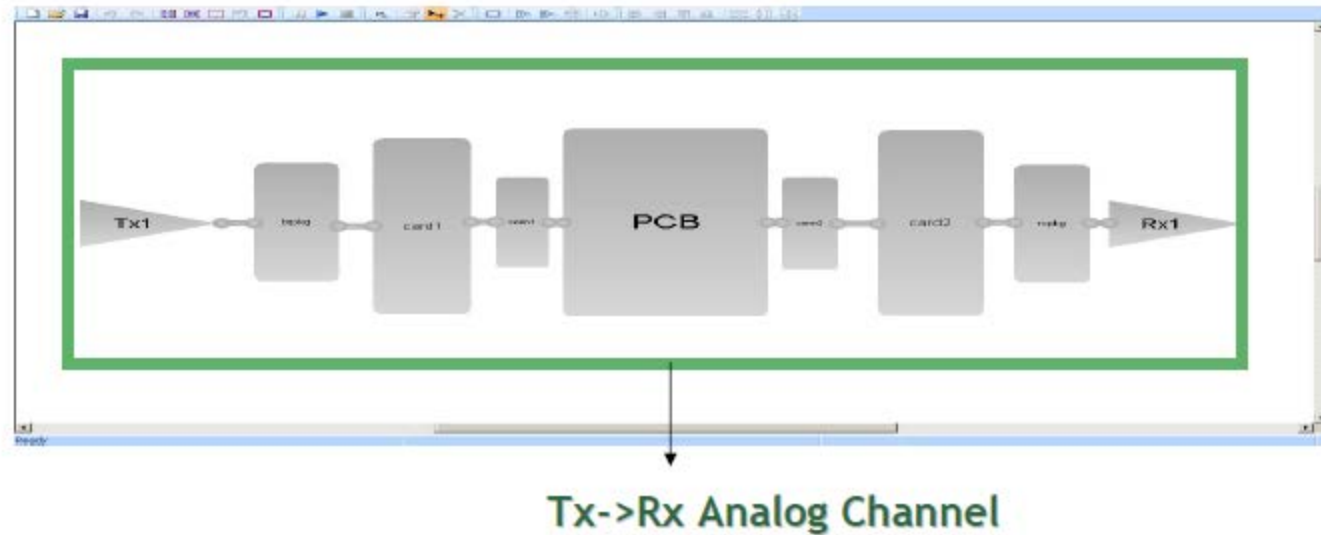
- Addressed device modeling challenges
- Enables pre Architectural level Exploration and post layout
- Already prevalent in IC design houses
- IBIS Version 5(Aug 2008) includes AMI Modeling support
- IBIS AMI Models are interoperable

# AMI – key concepts

- The Tx –to– Rx pathway is composed of 3 separate entities
  - Tx algorithmic part
  - The Analog channel
  - The Rx algorithmic part
- Three “decoupled” parts can be *independently* solved in time domain
- Executable model delivered as a dynamically linked library (DLL)
  - Data flow between these three parts is addressed by the standardized API
  - Robust and flexible parameter passing to Tx & Rx

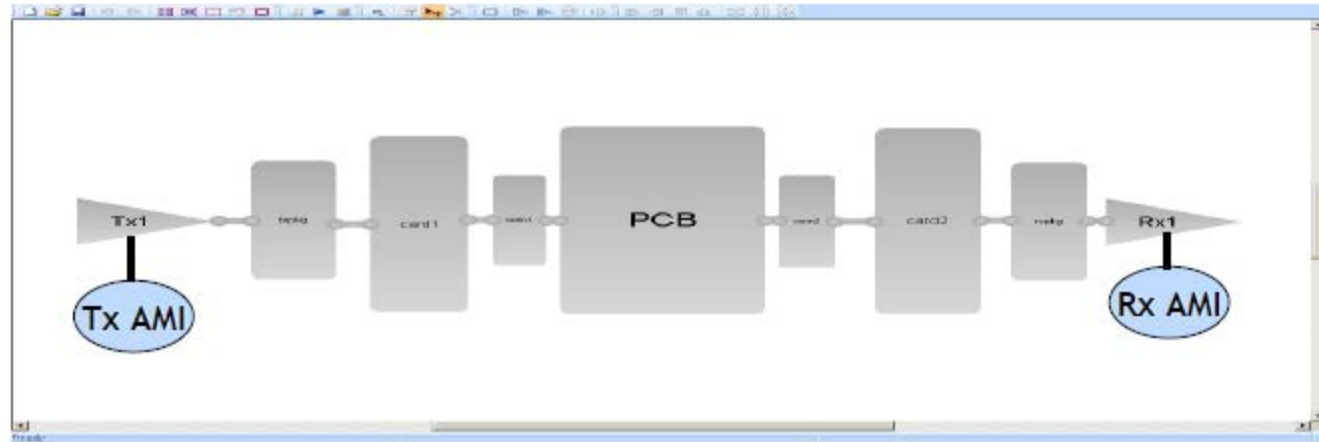


# IBIS AMI Analog Channel



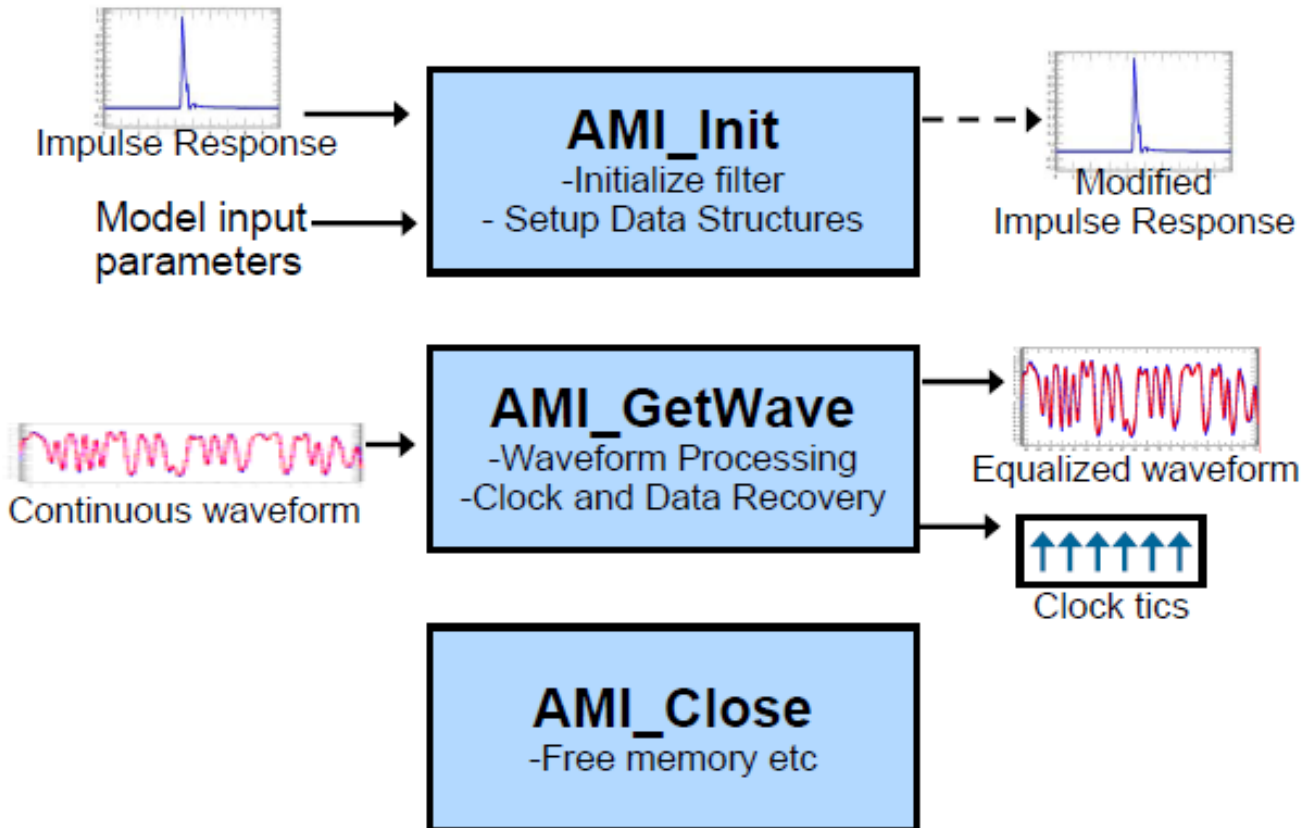
- EDA tools leverage/build on existing infrastructure
- Tx/Rx will still require an analog I/O front end model

# AMI Model Section



- AMI Models are Executable “blackbox”
- Platform dependent
- One AMI model/device
- Accompanied by Parameter Definition File

# IBIS AMI Data Flow API



# IBIS AMI-What it does and does not

## ■ Does

- How and what data is interchanged between eda tool and ic ami model during 'Init' and 'GetWave' call
- Pass the user settable parameters to the AMI model

## ■ Does not

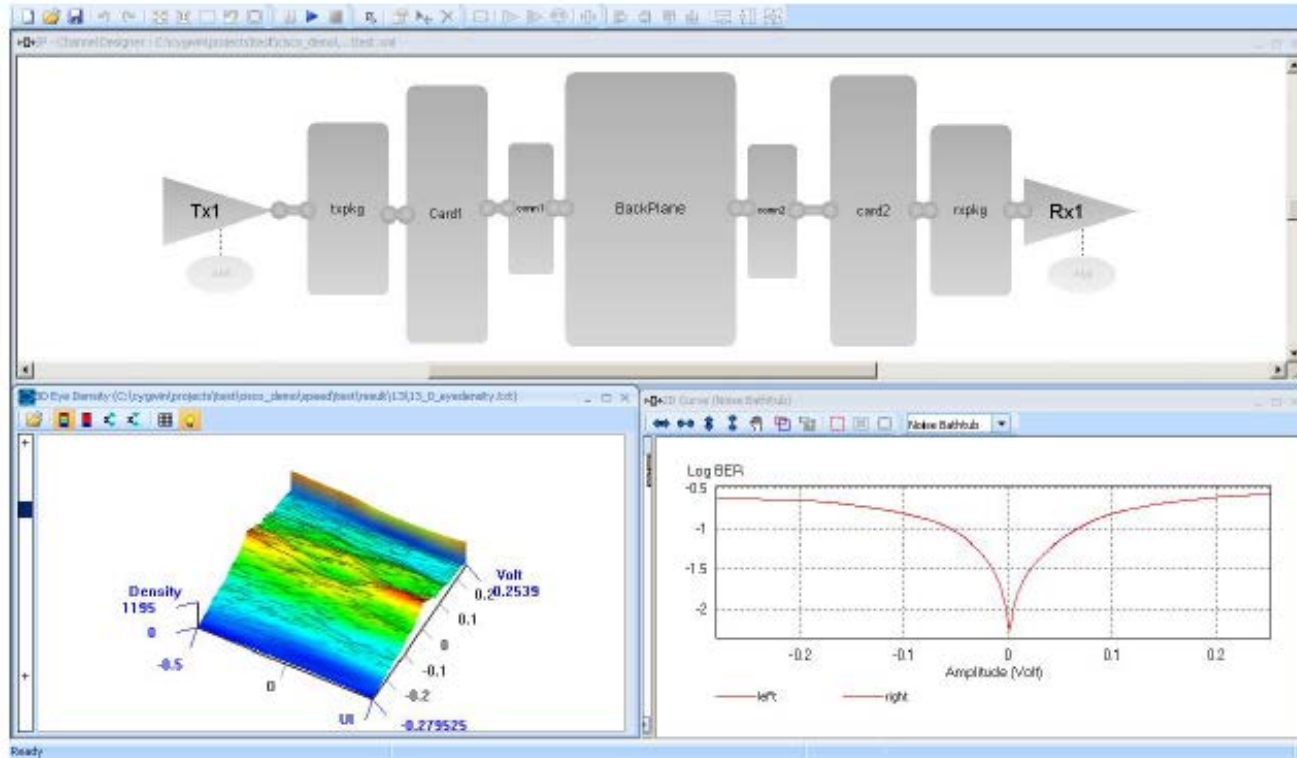
- Prescribe how the device has to be modeled
- State and limit the parameters which can be passed
- Specify how the eda tool should perform the simulation (Simulator Agnostic)
- Stipulate how eye diagram, Bit Error Rates have to be computed



# AMI Status

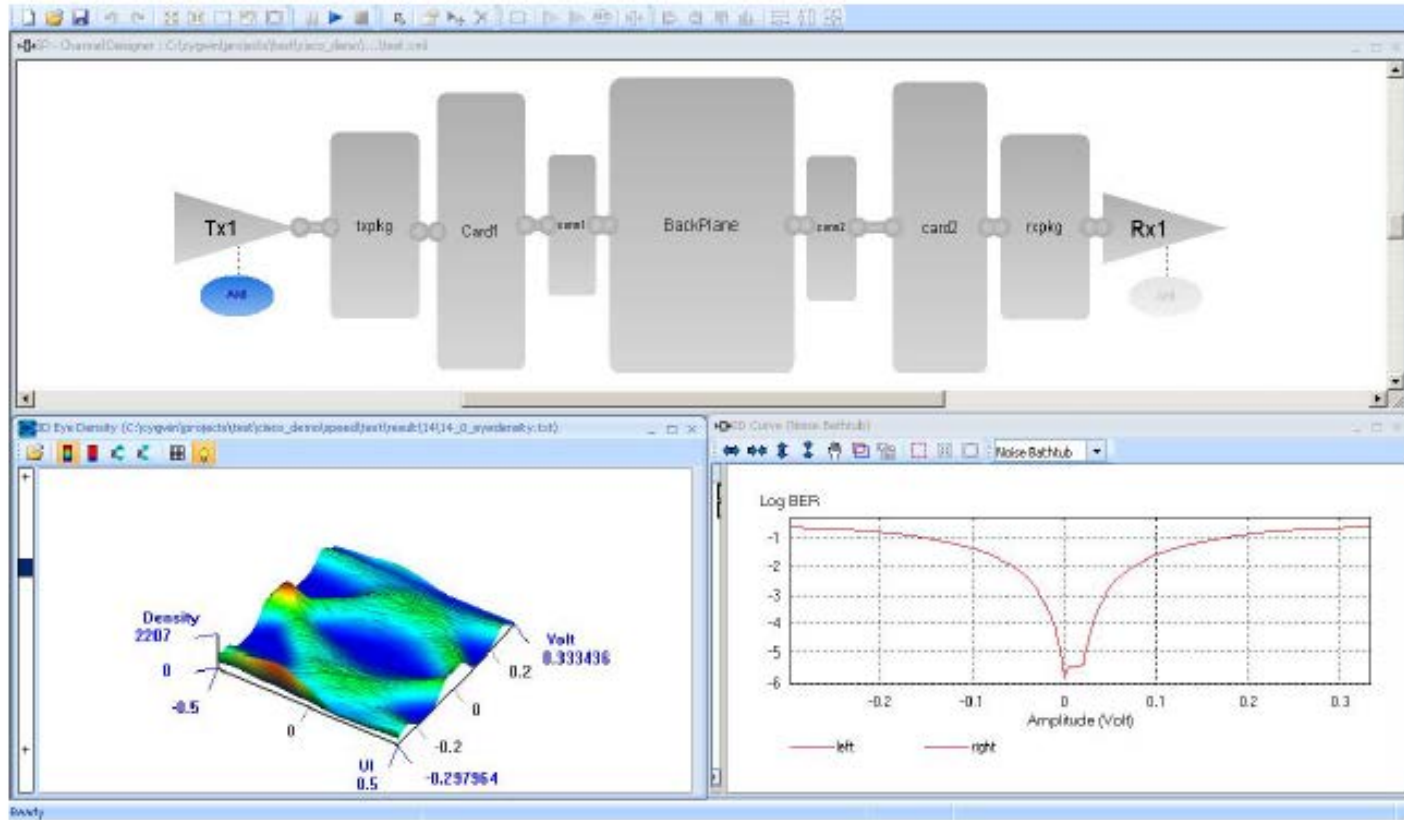
- AMI Models being developed and delivered by various ic vendors
- EDA tools need to support ami
- Models are available so far through nda

# AMI in action

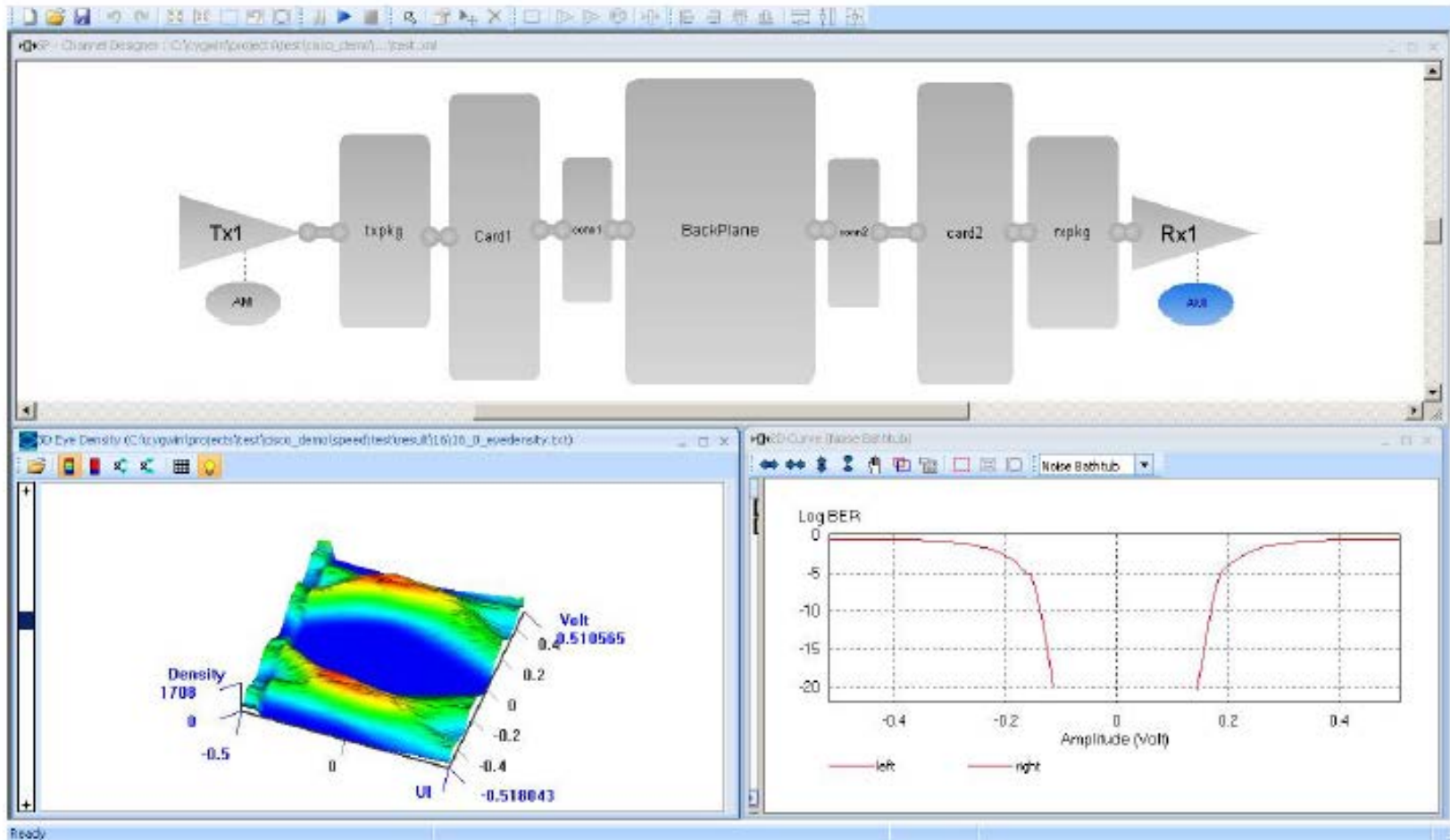


No AMI

# AMI FFE



# FFE + DFE



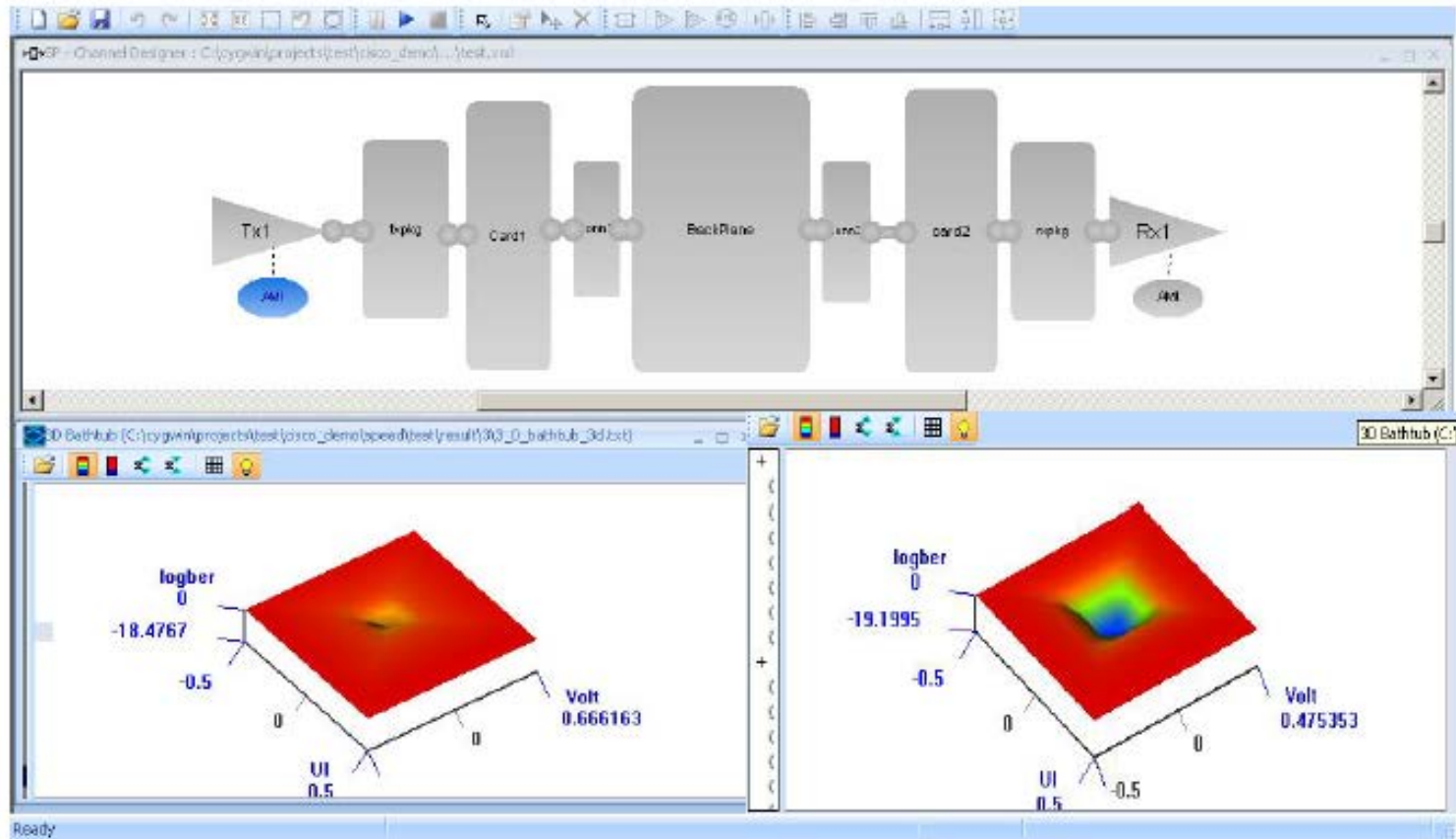
# AMI Models enable practical design space exploration

The screenshot displays the Channel Designer interface. The top part shows a signal path diagram with components: Tx1, bpk1, card1, conn1, BackPlane, conn2, card2, rxpk1, and Rx1. Below the diagram is the Sweeping Manager dialog box. The dialog is configured for AMI Parameters Sweeping with 4 total iterations. The parameter to be swept is 'pre:Tx1:amifc'. The results table shows the following data:

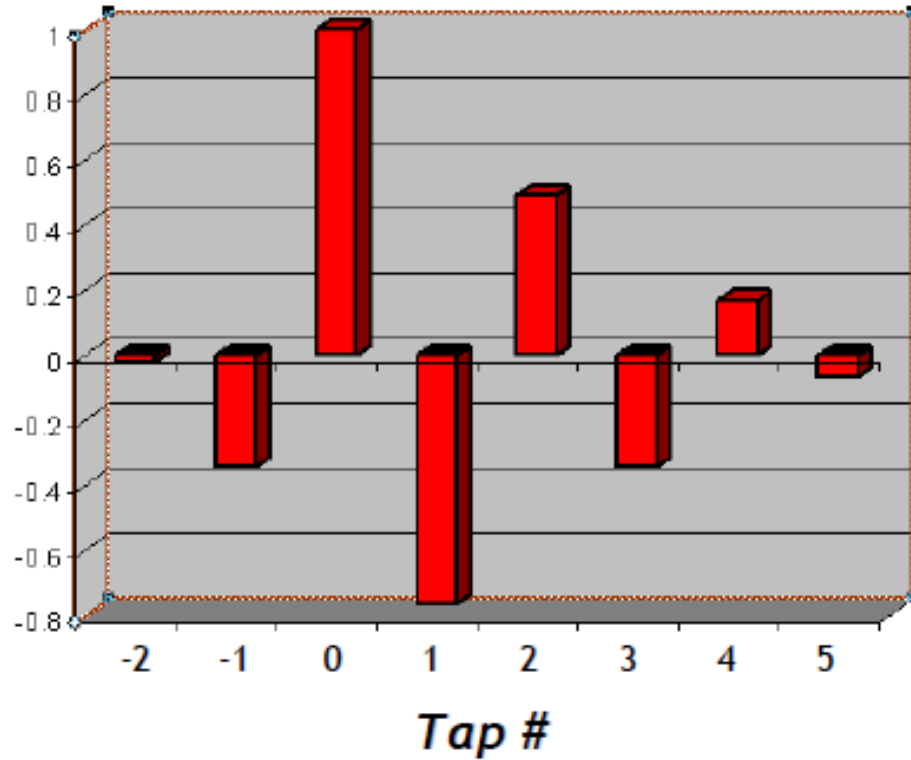
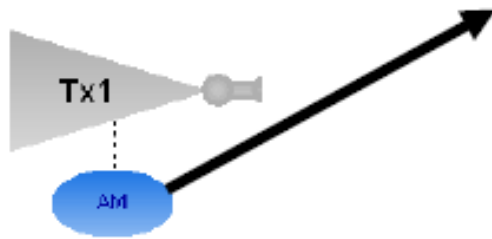
Iteration	Values	Time iter(UD)	Eye Height(mV)
1	pre:Tx1:amifc:0	0.56	218
2	pre:Tx1:amifc:1	0.12	365
3	pre:Tx1:amifc:2	0.12	356
4	pre:Tx1:amifc:3	0.12	477

Additional options in the Sweeping Manager include checkboxes for Eye Contour, Eye Density, Bathtub, and Report. The status bar at the bottom indicates 'Ready'.

# Design Space



# AMI optimizes tap coefficient



# Final Thoughts

- AMI Modeling is here
  - Essential for serial link analysis
- Pre and post layout
- Increasing model availability
- EDA tools support AMI



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