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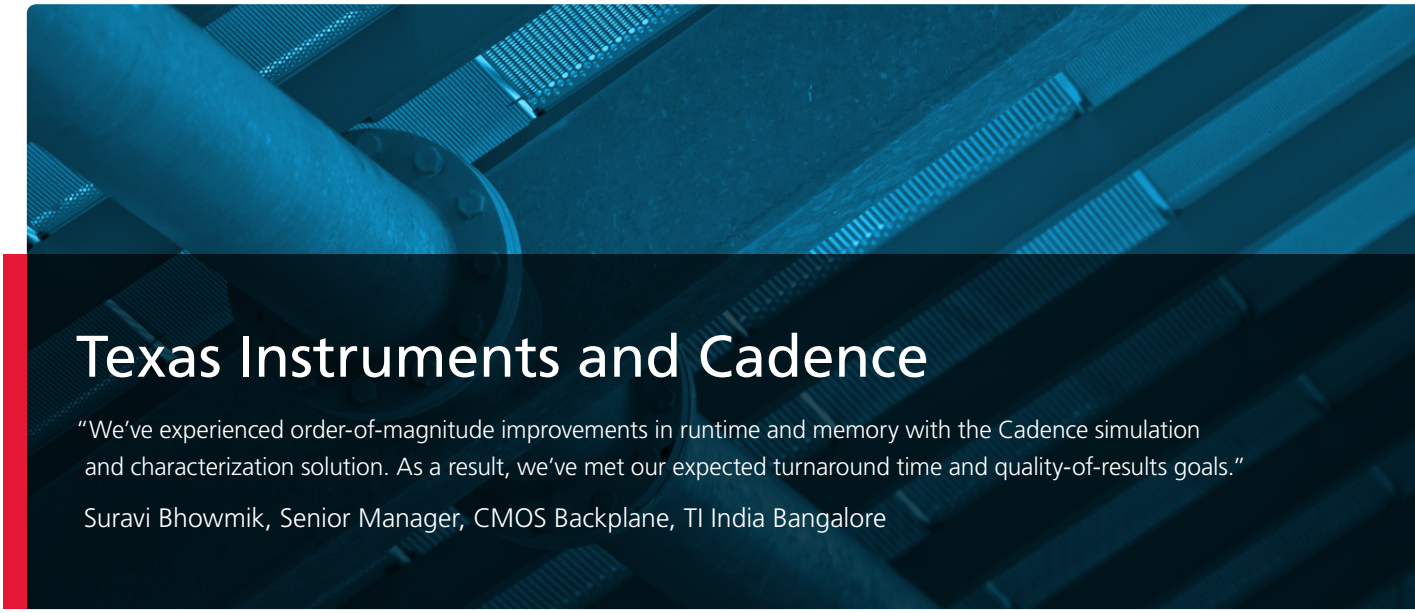

Texas Instruments and Cadence

"We've experienced order-of-magnitude improvements in runtime and memory with the Cadence simulation and characterization solution. As a result, we've met our expected turnaround time and quality-of-results goals."

Suravi Bhowmik, Senior Manager, CMOS Backplane, TI India Bangalore

The Customer

Texas Instruments (TI) is a global analog and digital semiconductor integrated circuit (IC) design and manufacturing company. In addition to developing analog technologies, digital signal processing (DSP), and microcontroller semiconductors, TI designs and manufactures semiconductor solutions for analog and digital embedded and application processing.

TI has a CMOS Backplane group in the External Development & Manufacturing (EDM) division in Bangalore, India. This group is responsible for electronic design automation (EDA) solutions and flow infrastructure for digital system-on-chip (SoC) designs and foundation intellectual property (IP). The company's Embedded Processing division, which includes the Microcontroller, Digital Signal Processing, OMAP, and Connectivity businesses, uses foundation IP developed by the EDM group, including standard cells, input/outputs (I/Os), and static random-access memories (SRAMs), to design their SoCs.

The Challenge

With today's increasing complexities in 40nm and lower nodes, one of the EDM team's biggest challenges is to speed the turnaround time for characterization of compiler memories while achieving the desired level of results accuracy. Increasing the memory footprint of the tools at these nodes for larger memory instances can also pose a problem, requiring expensive high-capacity machines for simulation and characterization.

"Every new technology node requires that we make a significant investment upfront in order to fine-tune runtime versus accuracy and achieve optimal tool settings for simulation and characterization," explains Suravi Bhowmik, senior manager, EDM, CMOS Backplane, TI India Bangalore.

Business Challenge

- Fast time to market and stringent quality and budget goals for SoC designs and foundation IP

Design Challenges

- Speed turnaround time for simulation and characterization of compiler memories
- Achieve desired level of results accuracy

Cadence Solutions

- Virtuoso Foundation IP Characterization
- Virtuoso Liberate MX
- Spectre XPS
- Spectre APS

Results

- Achieved full SRAM simulation for today's SoC timing and leakage and static power requirements
- Achieved a 2X reduction in characterization cycle time compared to previous solution
- Met quality-of-results goals

"Runtimes of the simulator and characterization tools have increased with every new process node, especially with the need for accurate leakage and dynamic (internal) power requirements in addition to timing requirements," she continues. "Tool stability is also key to ensure predictable execution and cycle times."

Together, these challenges lead to overall increased development cost and cycle time for compiler memories.

The Solution

After researching several solutions on the market and trying another product for one year with inadequate results, the TI EDM team began to explore a complete Cadence® characterization solution including Cadence Virtuoso® Foundation IP Characterization, Cadence Spectre® Extensive Partitioning Simulator (XPS), and Cadence Spectre Accelerated Parallel Simulator (APS). The team members decided that this uniquely integrated simulation and characterization solution was best suited to help them meet the challenges involved with advanced nodes and low-power architecture.

> *"This complete Cadence solution enables increased throughput and quality, while maintaining the level of SPICE accurate results where required. It provides the breakthrough we need to deliver the required capacity and performance of today's low-power and high-performance, advanced process node, post-layout SRAM designs."*

Virtuoso Foundation IP Characterization delivers the industry's most complete, robust solutions for the characterization and validation of foundation IP from standard cells, standard I/Os, complex I/Os, and memories. Patented "Inside-view" technology originally from Altos delivers faster time to market and better correlation to silicon by improving library throughput and ensuring timing, power, noise, and statistical coverage of cells. Spectre XPS is the next generation FastSPICE simulation technology built on top of Cadence's well established Spectre architecture that covers SPICE, advanced SPICE, and now the latest FastSPICE technology available on the market.

Specifically, the TI EDM team adopted three products from this solution: Cadence Virtuoso Liberate MX, Cadence Spectre XPS, and Cadence Spectre APS. Virtuoso Liberate MX is the memory characterization tool that controls the simulations, Spectre XPS is the fastSPICE simulation technology that simulates the entire design, and Spectre APS is used to perform accurate simulation runs on smaller portions of the design.

"This complete Cadence solution enables increased throughput and quality, while maintaining required level of SPICE accuracy. SPICE accurate results where required," Bhowmik says. "It provides the breakthrough we need to deliver the required capacity and performance for today's low-power and high-performance, advanced process node, post-layout SRAM designs."

Virtuoso Liberate MX extends the Cadence solution's standard cell and I/O library characterization capabilities to cover larger macro blocks, such as memory and custom cores. Macro blocks require additional pre-analysis steps in order to achieve fast and accurate characterization and meet chip performance and power-consumption goals. To validate a design's electrical performance, it's essential to have a highly accurate electrical model for each macro equivalent in accuracy to the electrical models used for standard cells and I/Os.

Spectre XPS provides the capacity and performance the EDM team required to meet and exceed its solution requirements. This next-generation fastSPICE simulation technology is able to take in parasitics, handle low-power architectures, and still deliver performance where previous-generation fastSPICE simulation technology falls short.

"With this Cadence solution, we're able to deliver performance with complex power structures, and we're able to deliver accurate leakage and dynamic power measurements," Bhowmik says.

In addition to providing the right solutions, Cadence provided the right support services for this TI team.

"The Cadence R&D team members provided outstanding support during the entire engagement," Bhowmik says. "They were proactive in understanding our requirements and responding with aggressive schedules to meet our timelines."

Results

"We've experienced order-of-magnitude improvements in runtime and memory with the Cadence simulation and characterization solution," Bhowmik continues. "As a result, we've met our expected turnaround time and quality-of-results goals."

With the Cadence solution, the TI EDM team achieves full SRAM simulation for the timing, leakage, and static power requirements that are critical for today's SoCs. The team achieved a 2X reduction in characterization cycle time compared to the previous solution.

"We never had to compromise our desired level of accuracy, which translated into better quality," Bhowmik adds. "Another less-obvious benefit is that we enabled the simulation of very large embedded memories. Our customers can now look at the variation of their designs and the impact on different performance metrics."

Summary and Future Plans

Cadence advanced simulation and characterization solutions helped the TI EDM team meet its cycle-time and capacity requirements for compiler memory design, verification, and characterization.

Moving forward, TI will use the Virtuoso Liberate MX, Spectre XPS, and Spectre APS solution for compiler memory design and characterization across all technology nodes. This solution will soon be deployed to production.

"It has been an extremely fruitful experience using the Cadence solution and working with the Cadence R&D team, and we look forward to continuing this relationship," Bhowmik concludes. "With Cadence, we're meeting our goal to accelerate memory characterization. The R&D team is extremely motivated and proactive in understanding our requirements and helping us achieve our goals within very aggressive timeframes."

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