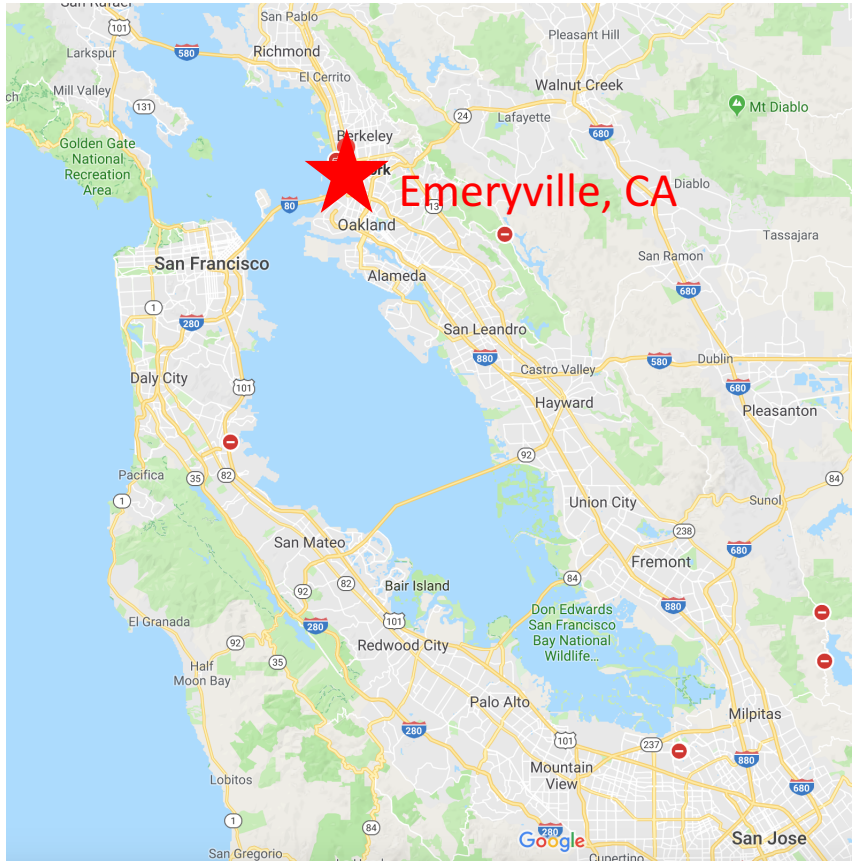
Ayar Labs

Building Photonics with Standard CMOS Platforms

Mark Wade — President and Chief Scientist

11/7/18

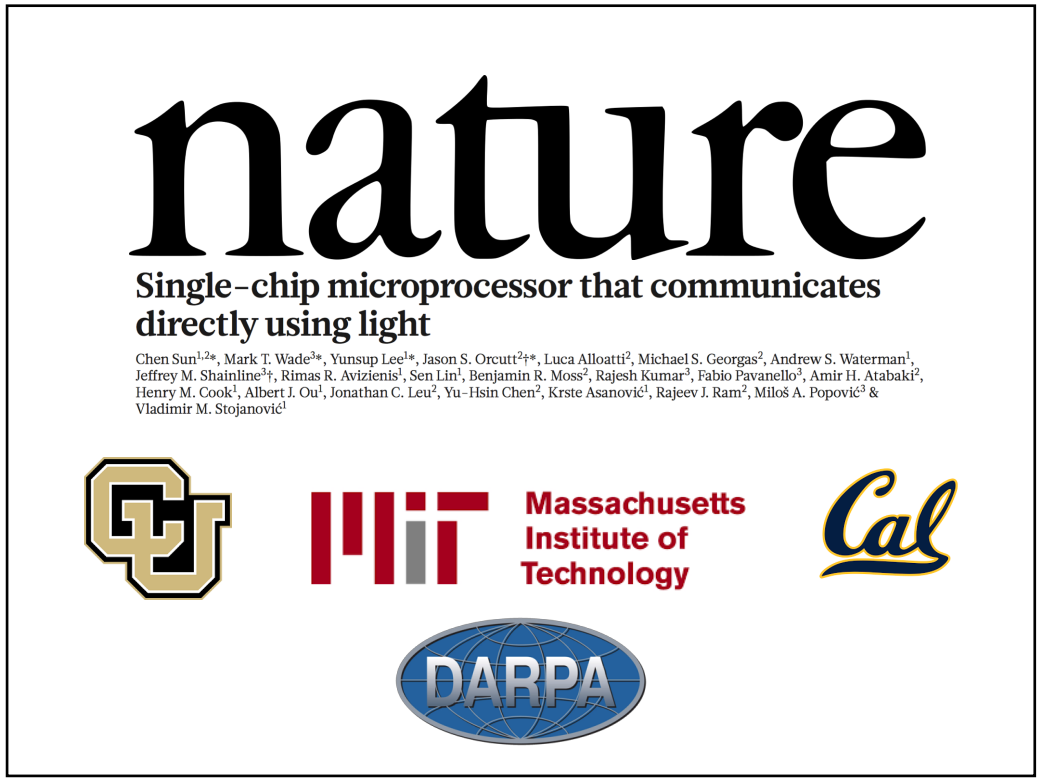
Company overview



- Based in Emeryville, CA (right next to Berkeley, CA)
- VC backed company
- ~15 people right now, but we're hiring!

Ayar Labs Background

- Based in Emeryville, CA (right next to Berkeley, CA)



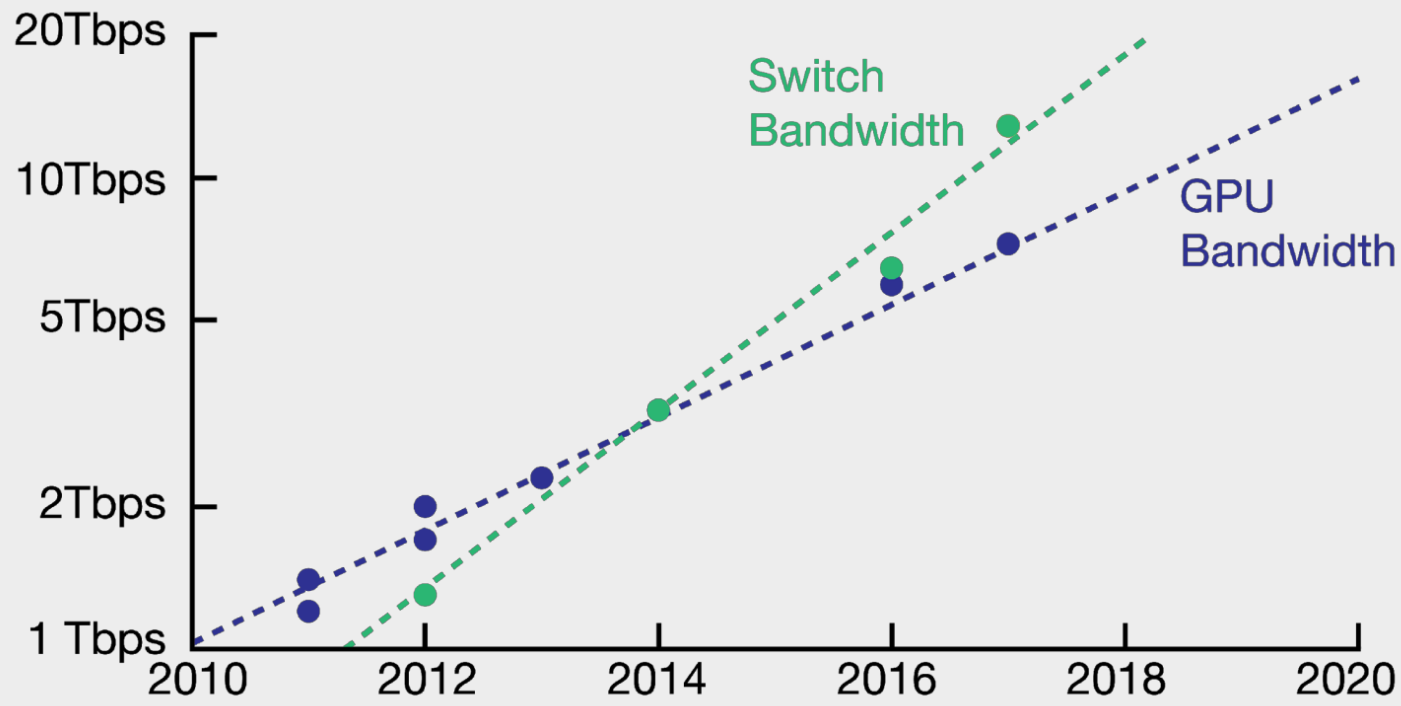
2015

Ayar Labs

Outline

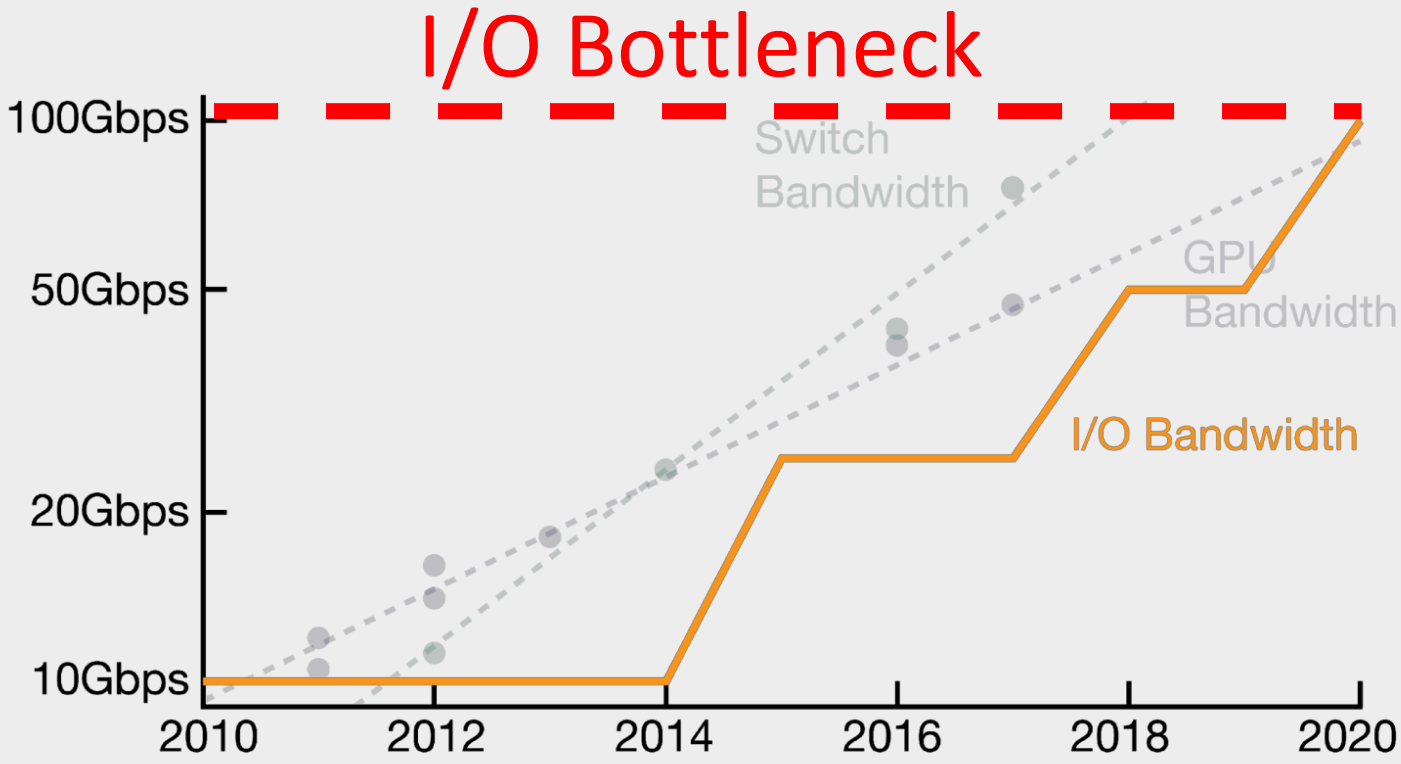
- Introduction and motivation
- Photonics in SOI CMOS
- Photonics in Bulk CMOS

ASIC bandwidth is growing



Sources: Product spec sheets. Data available upon request.

But electrical I/O is at its limit



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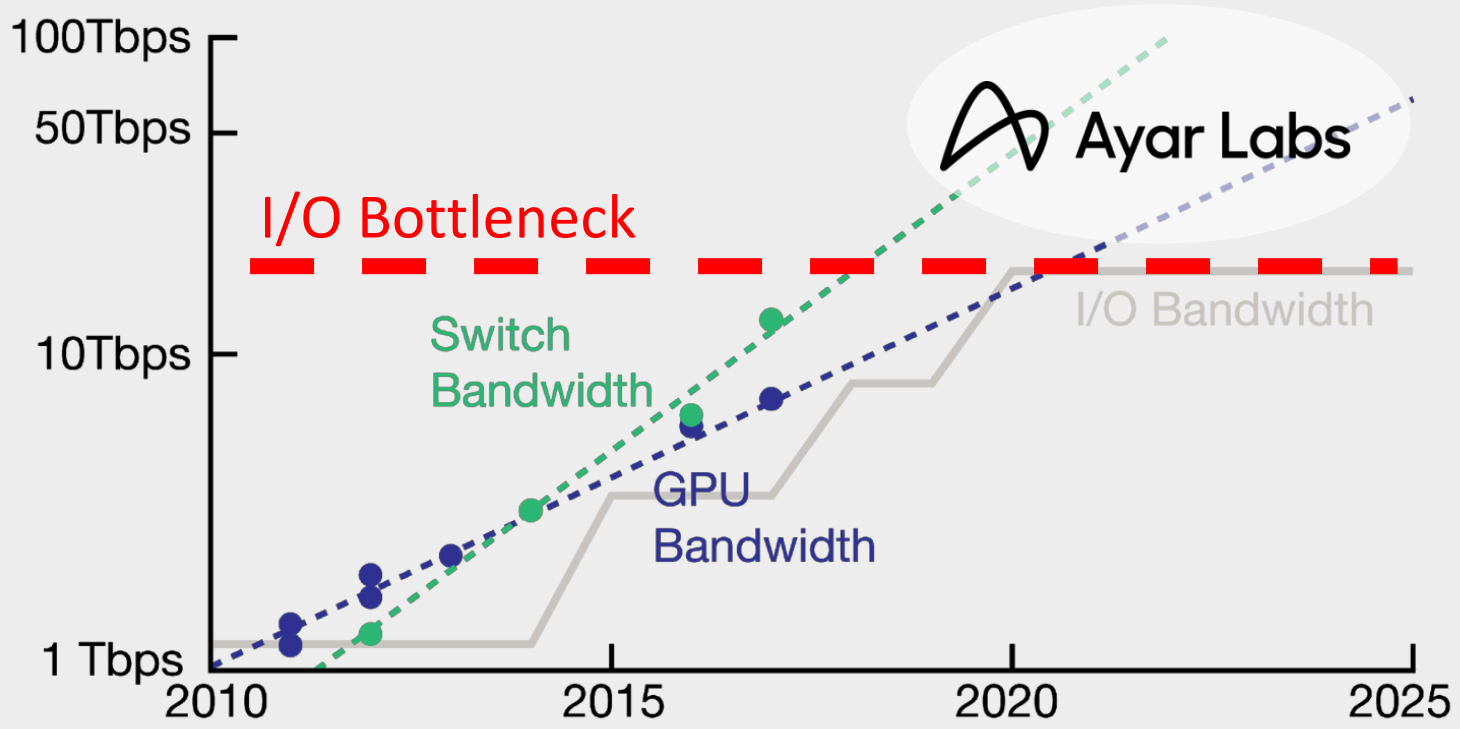
>2020 product roadmaps need a new solution



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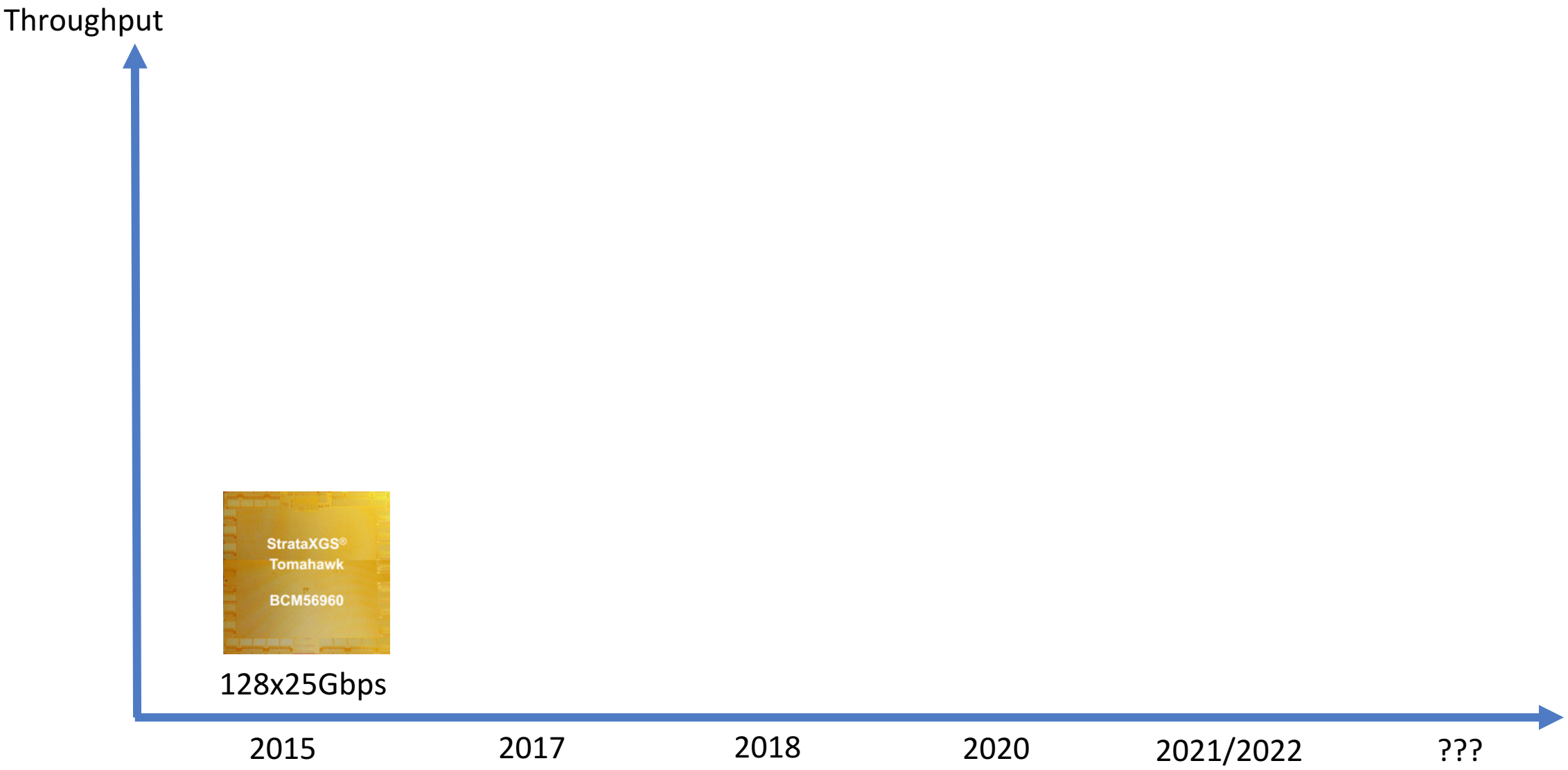
Switch Scaling: Growing Pains



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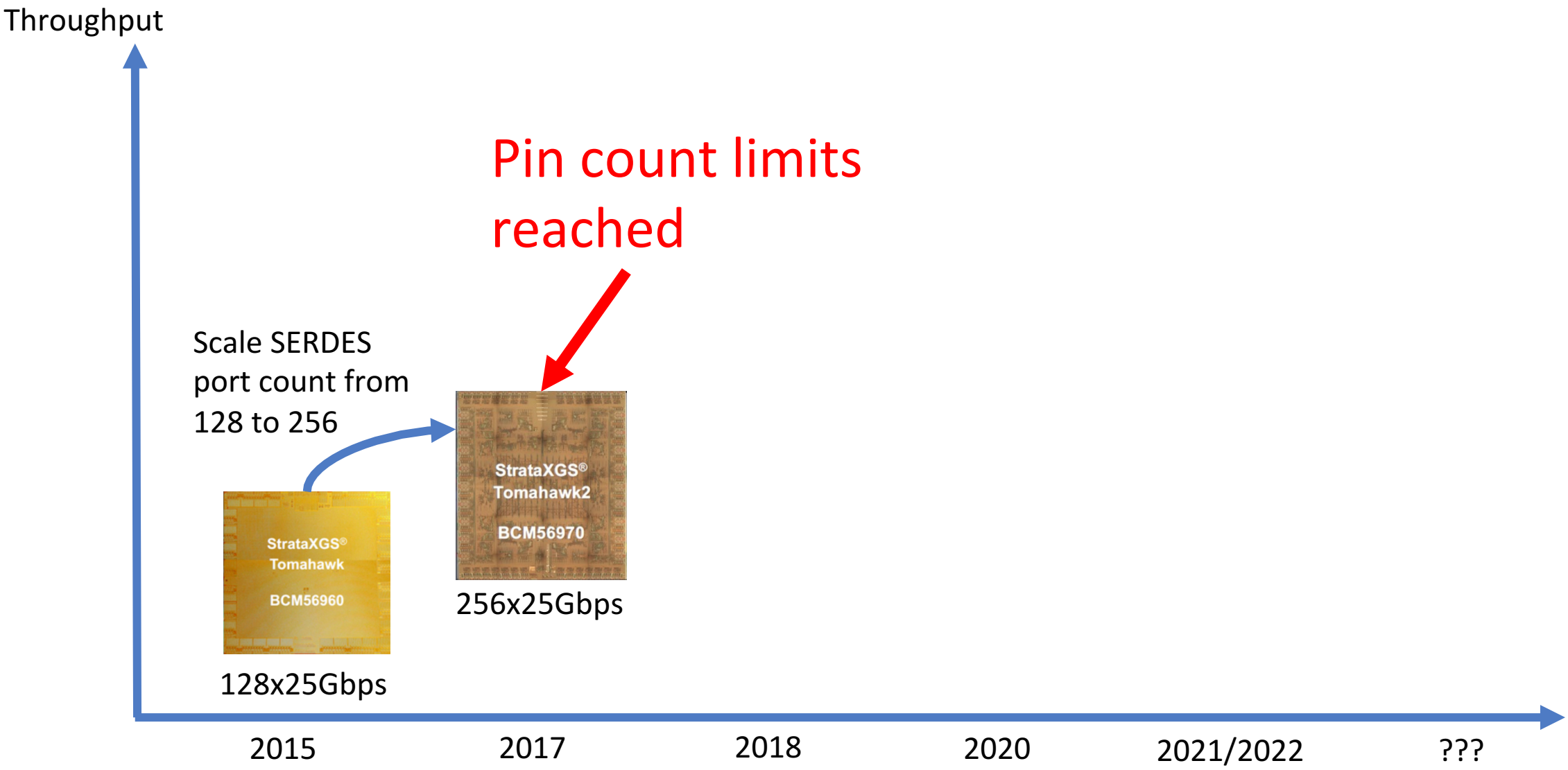

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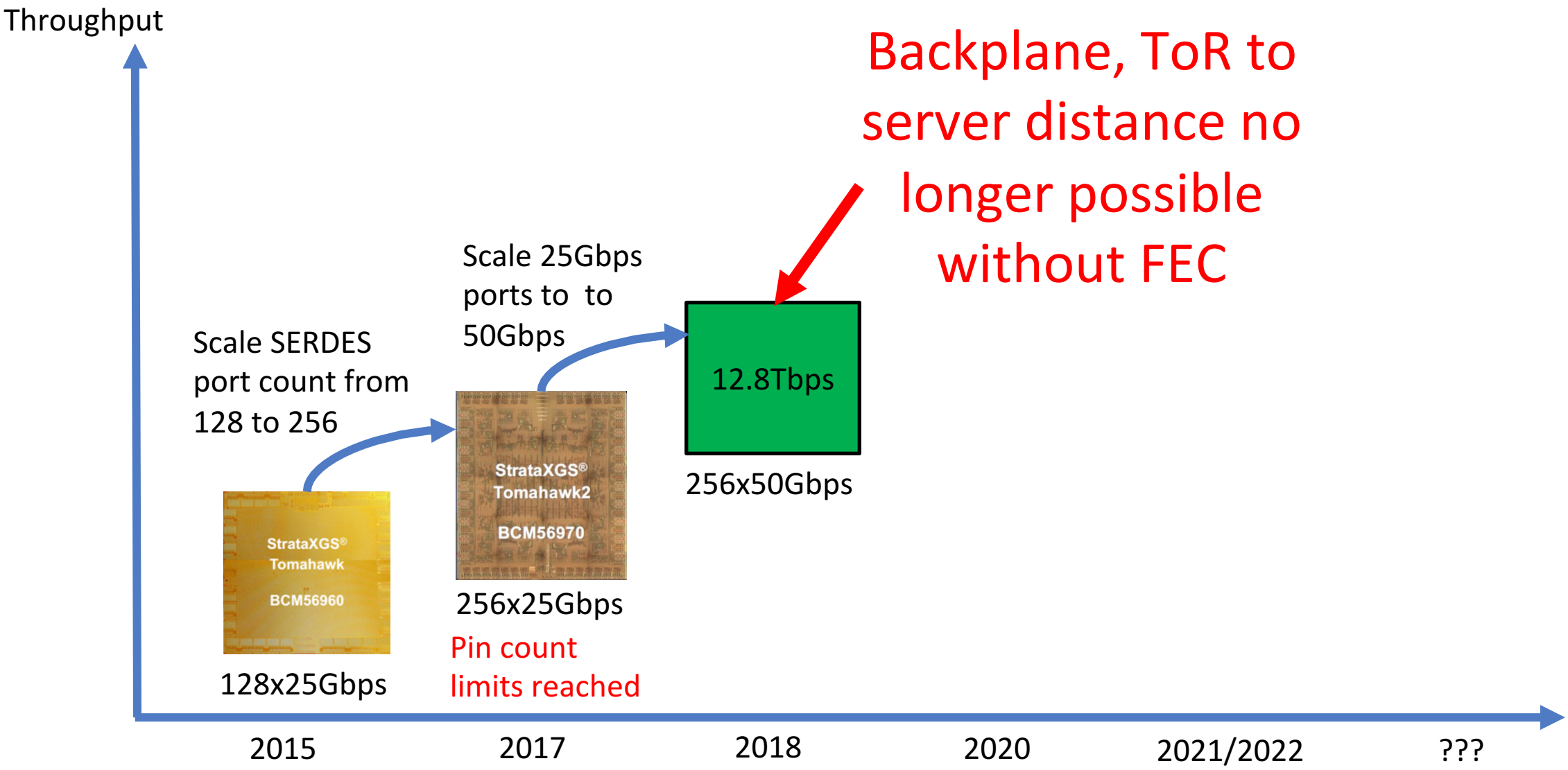

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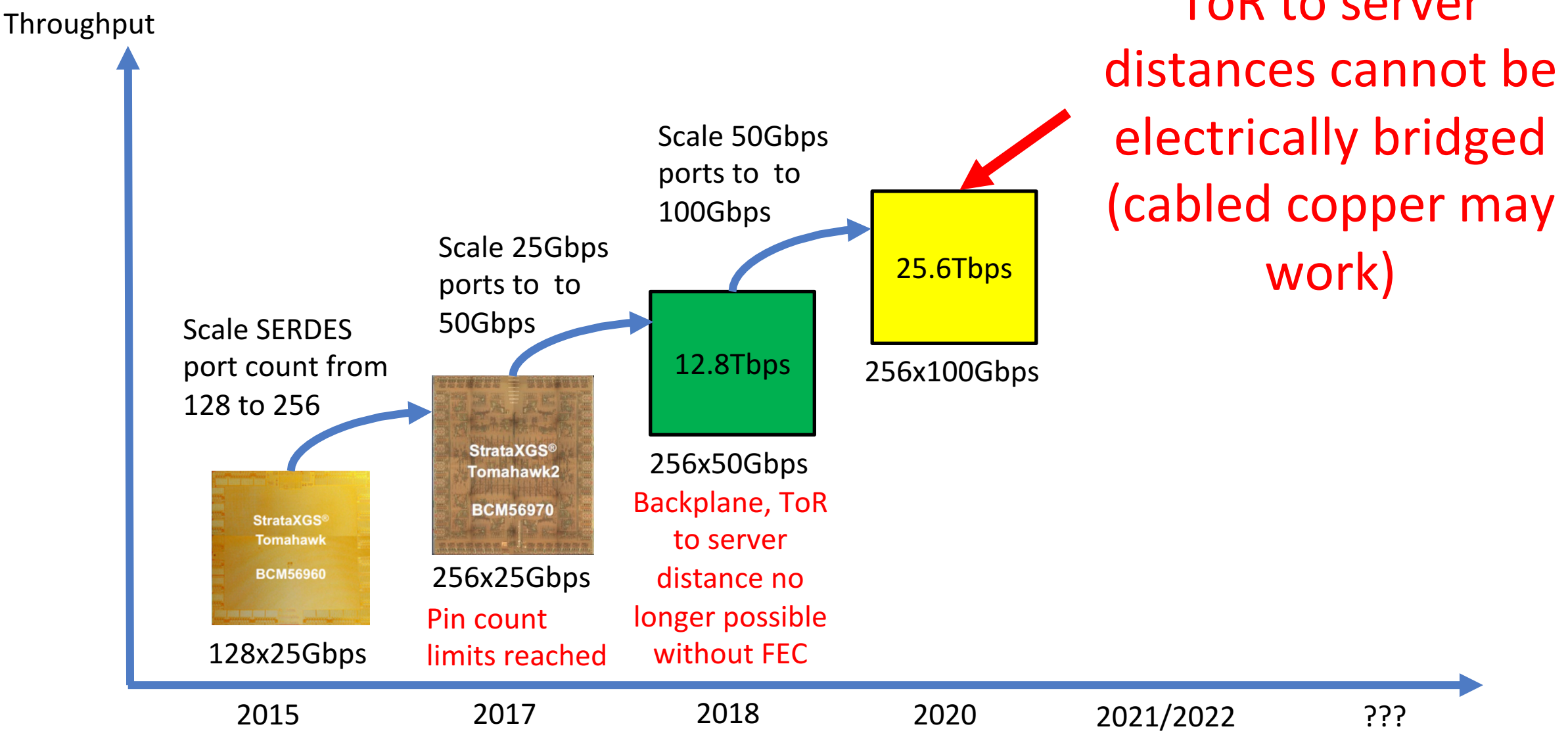
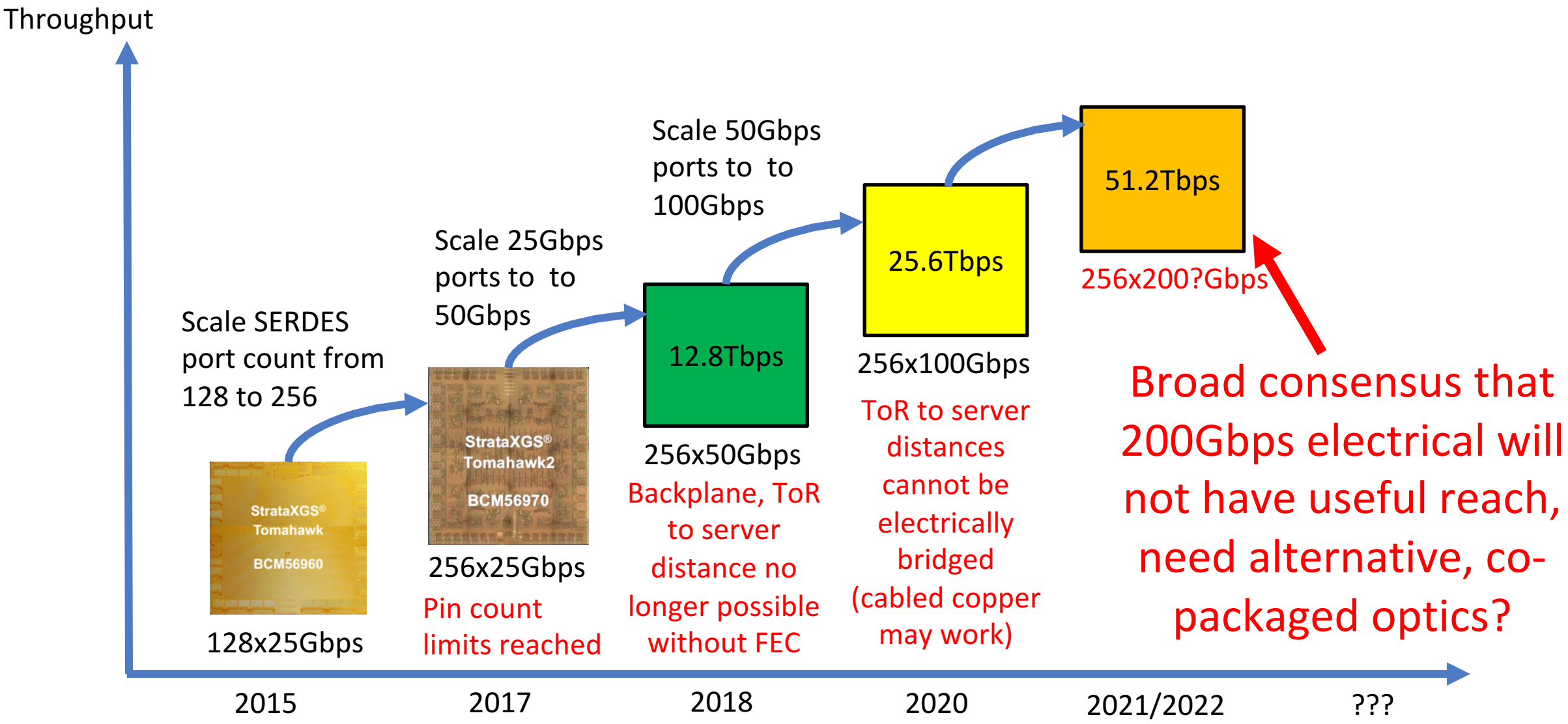


ToR to server distances cannot be electrically bridged (cabled copper may work)

Switch Scaling: Growing Pains



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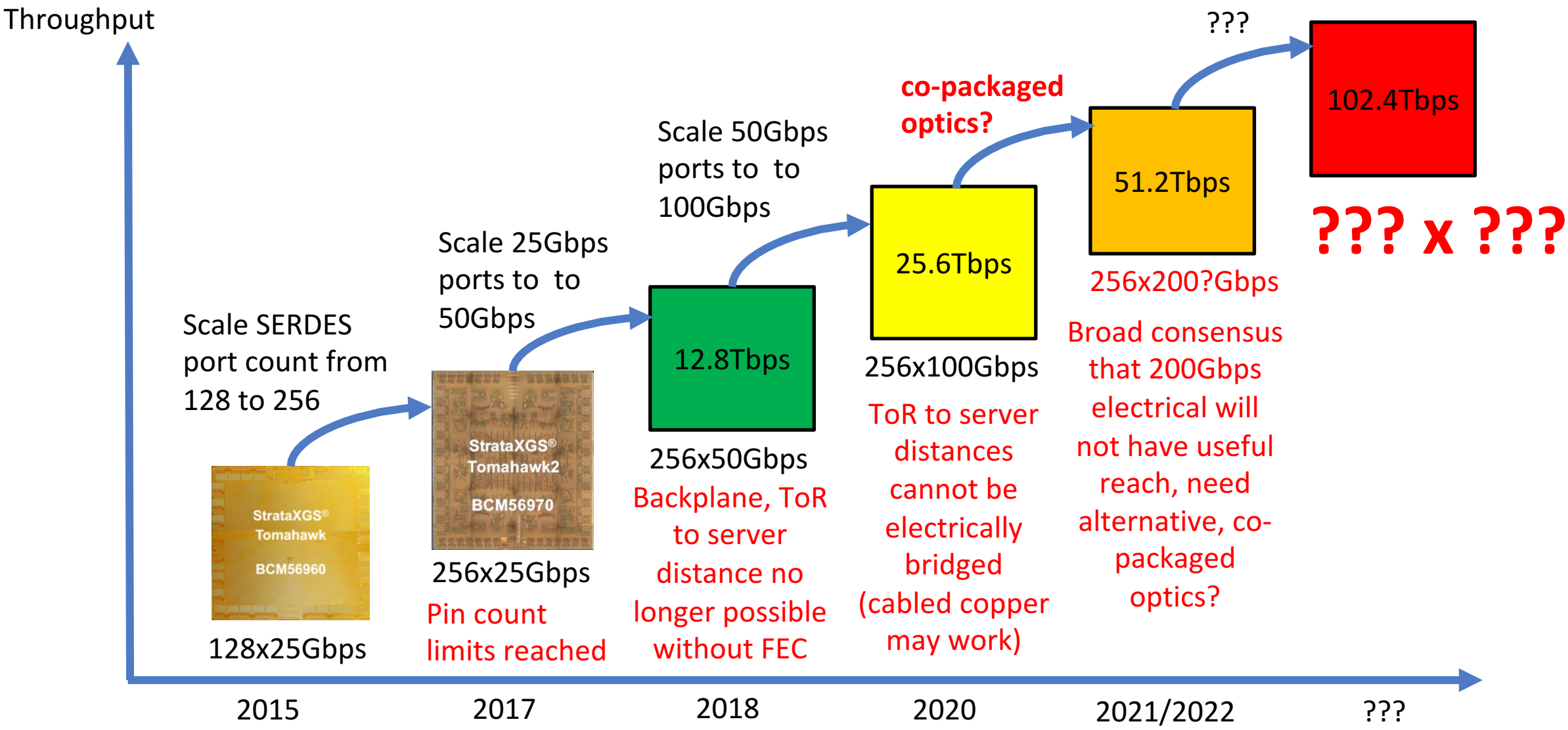
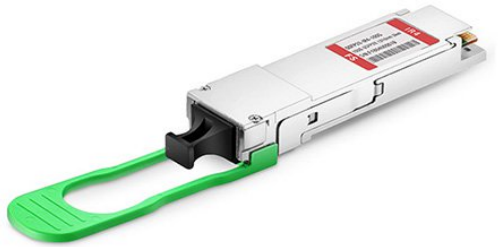
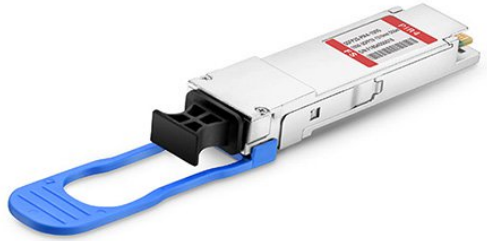


A new era of optics

100G Pluggables



Next-Gen 400G Pluggables



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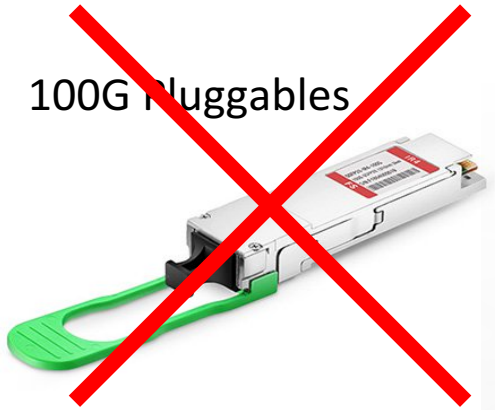

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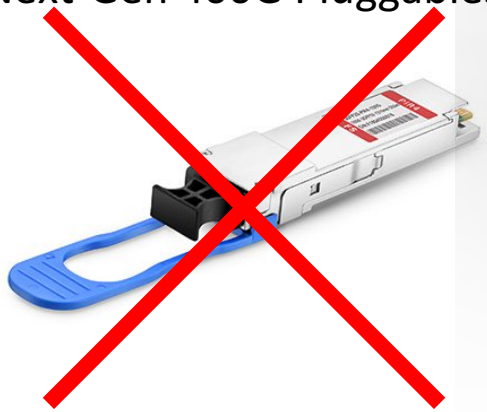
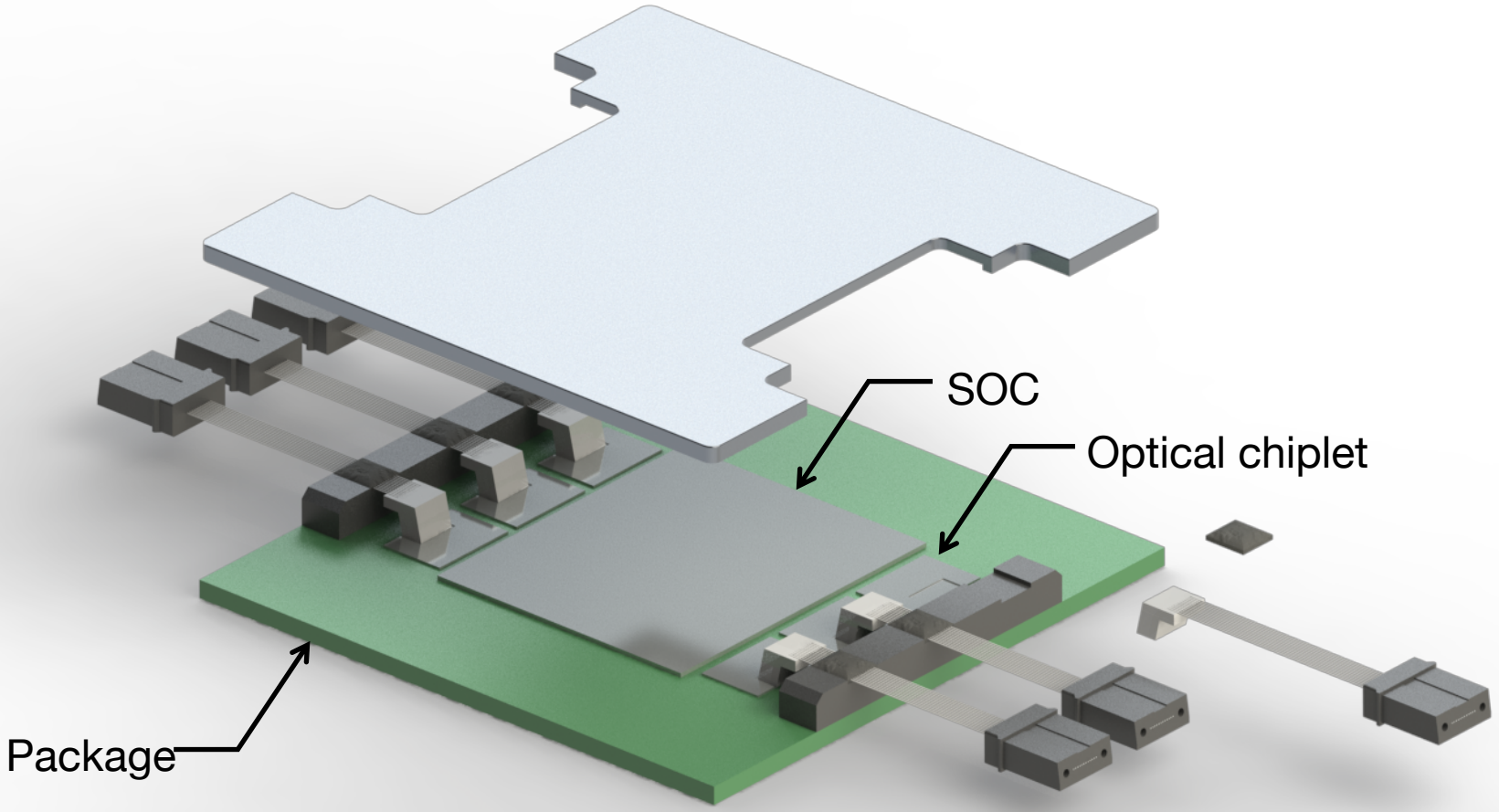
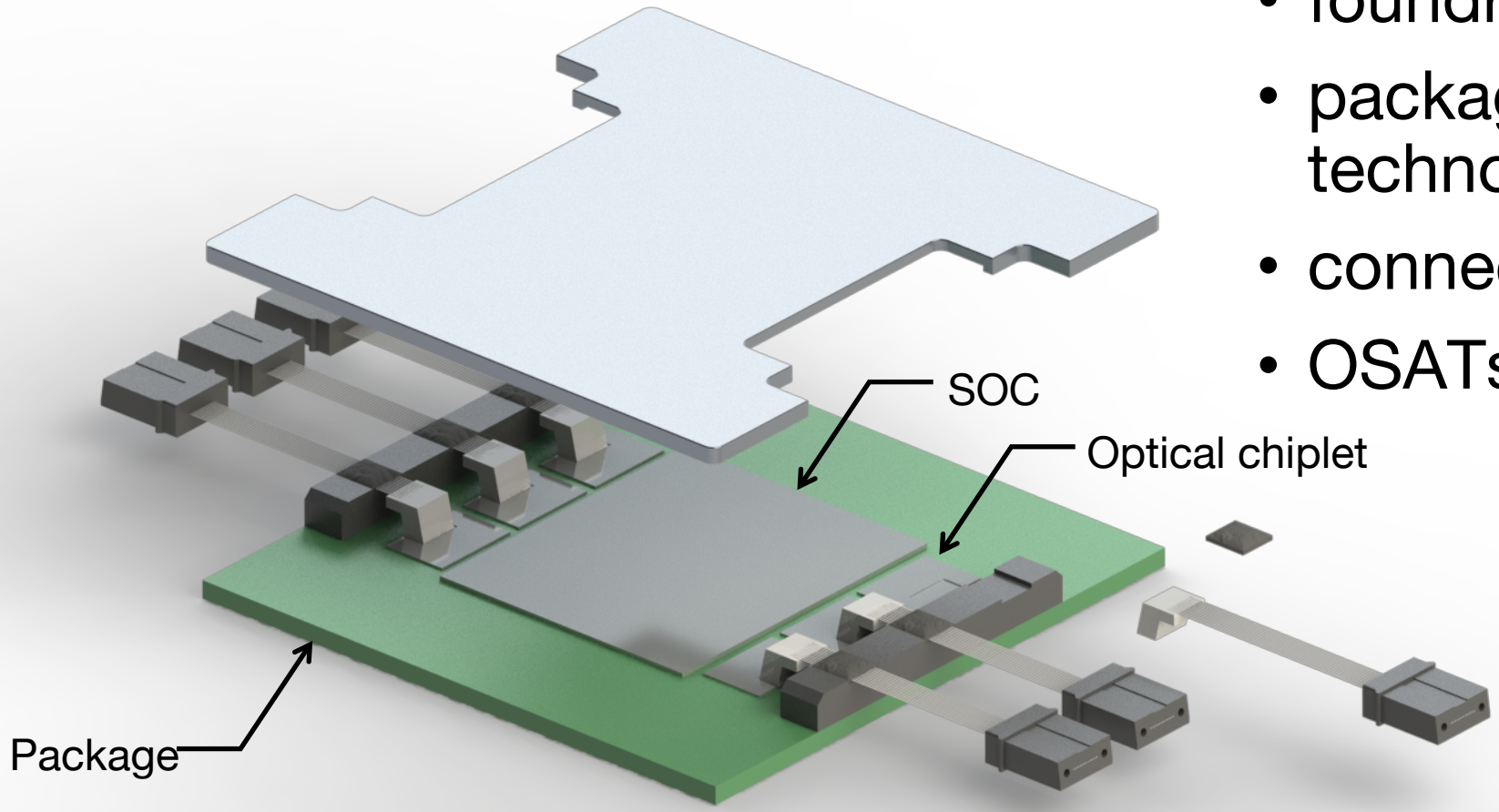




A new era of optics

- electronic-photonic packages
- requires an ecosystem:
  - foundries
  - package/assembly technologies
  - connector vendors
  - OSATs

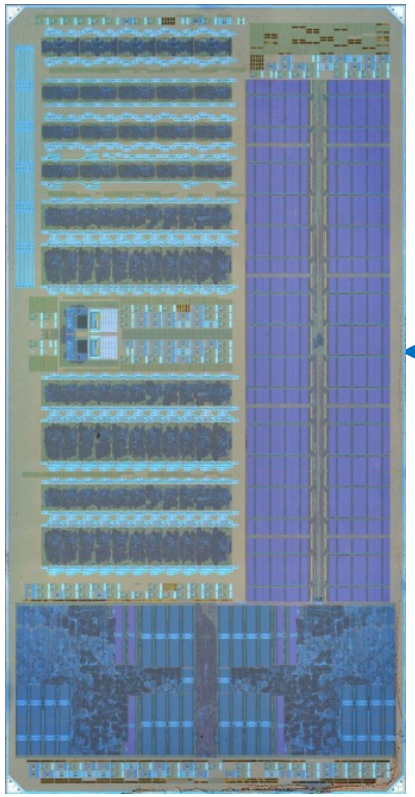


High volume markets will drive follow-on opportunities

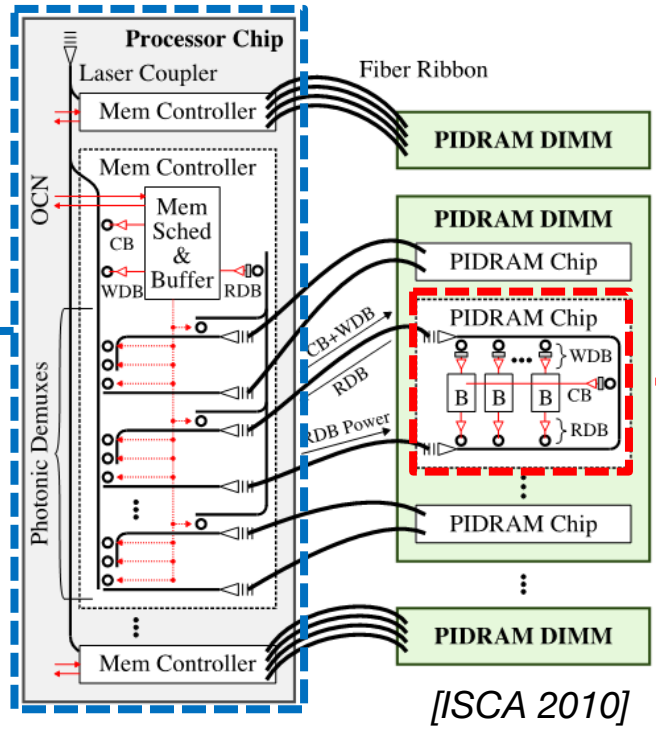
- Optical I/O
  - drives investment in ecosystem:
    - advanced foundry integration, PDKs, packaging, OSATs, ...
- Once the ecosystem is established, follow-on opportunities can be addressed
  - sensing
  - imaging
  - free-space communications
  - quantum computing

Photonic processor to memory interconnect

High Performance 45nm SOI



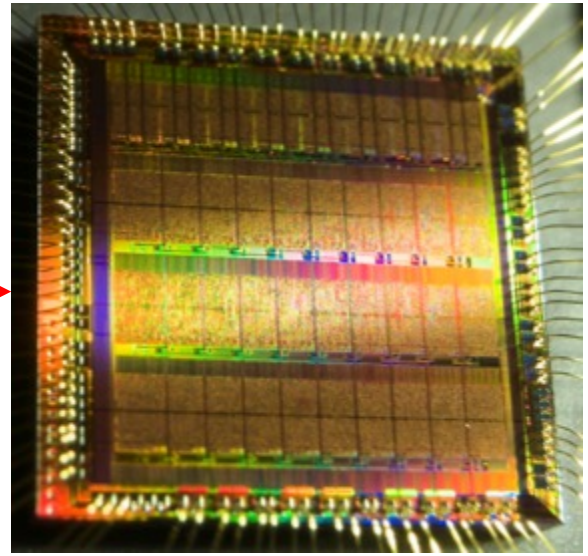
70M transistors
1000 optical devices



[ISCA 2010]

DARPA POEM

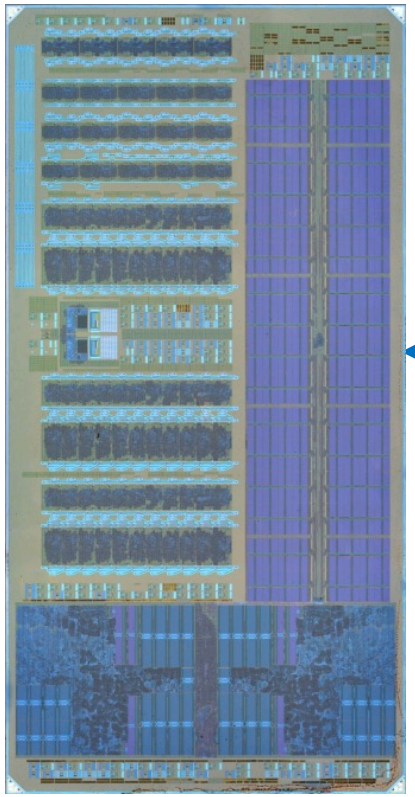
0.18µm Bulk



2M transistors
1000s optical devices

Photonic processor to memory interconnect

High Performance 45nm SOI



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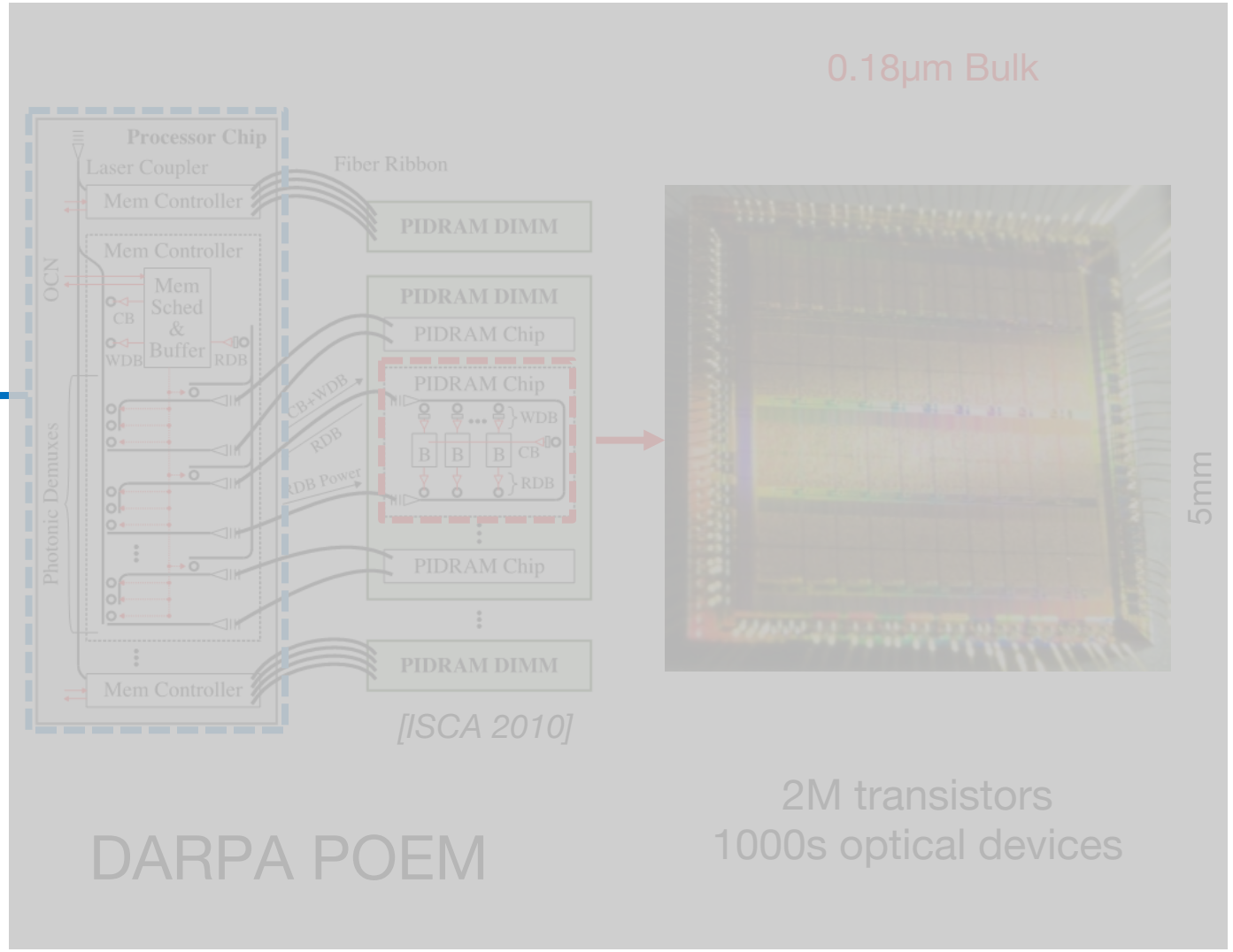

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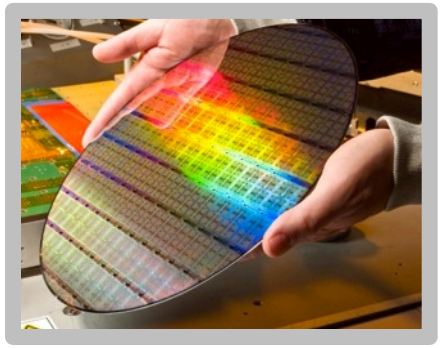
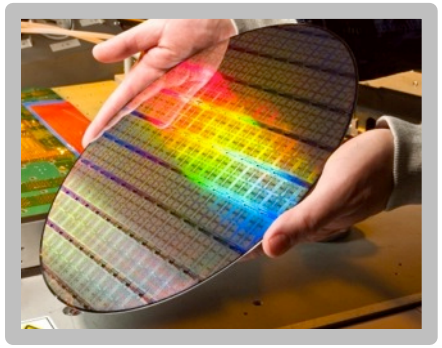
“Zero-Change” approach to integration: 45RFSOI



- 300mm wafer, commercial process

“Zero-Change” approach to integration: 45RFSOI



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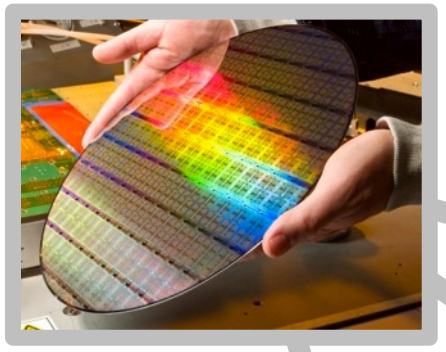
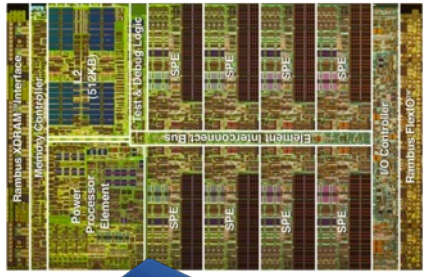
“Zero-Change” approach to integration: 45RFSOI

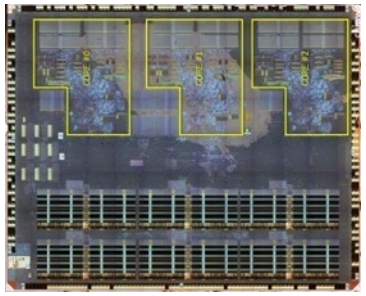


- 300mm wafer, commercial process
- Qualified, high-volume production since 2008
- Advanced process used in microprocessors
  - N-FET transistor f_T = 485 GHz [Lee, IEDM 2007]
- Photonic enhancement enables VLSI photonic systems

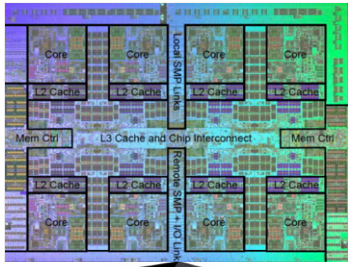
IBM Cell

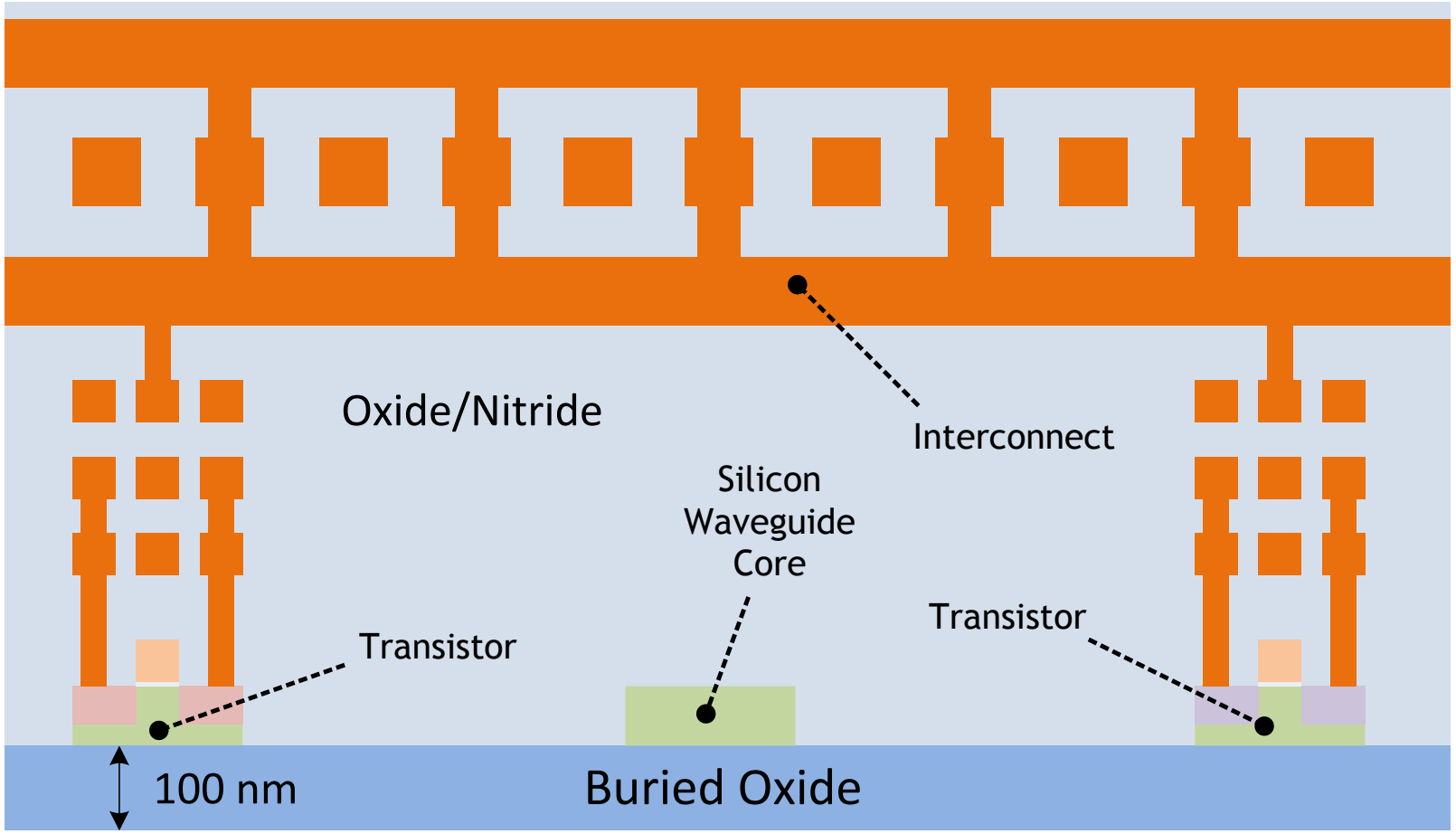


IBM Espresso



IBM Power7

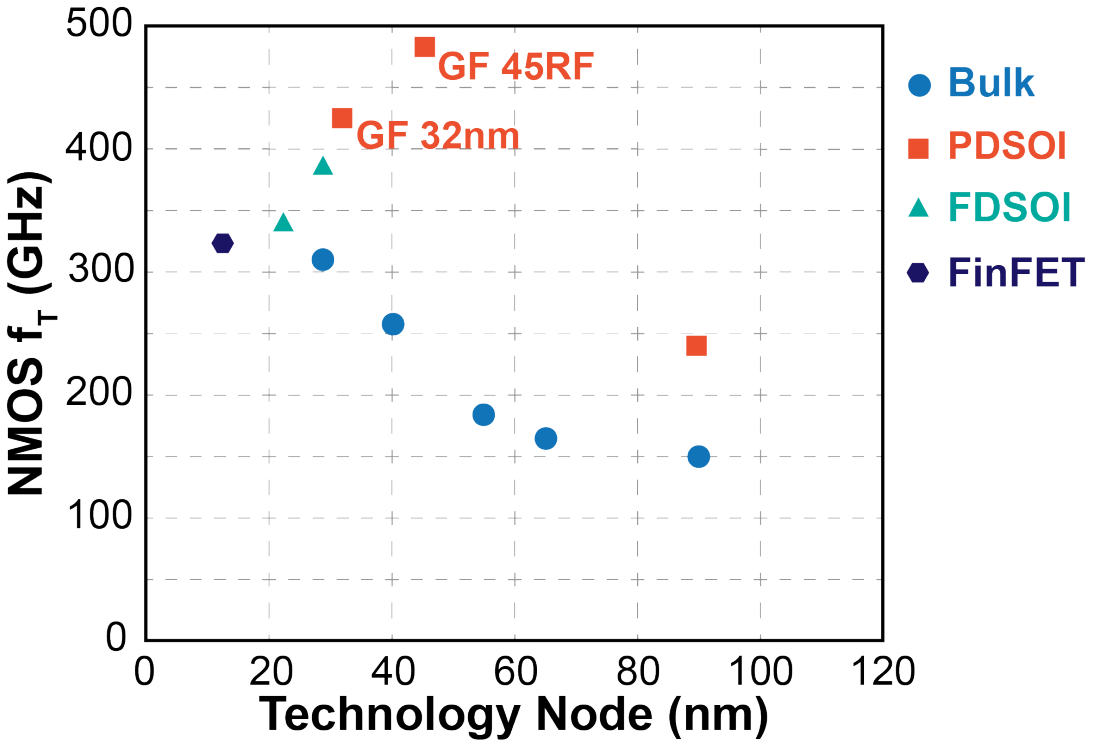




Air

[Orcutt Opt. Ex. 2012]

Why is 45nm SOI special?



[Stojanovic, Opt. Ex 2018]

- Transistor performance comparable or exceeding leading-edge nodes

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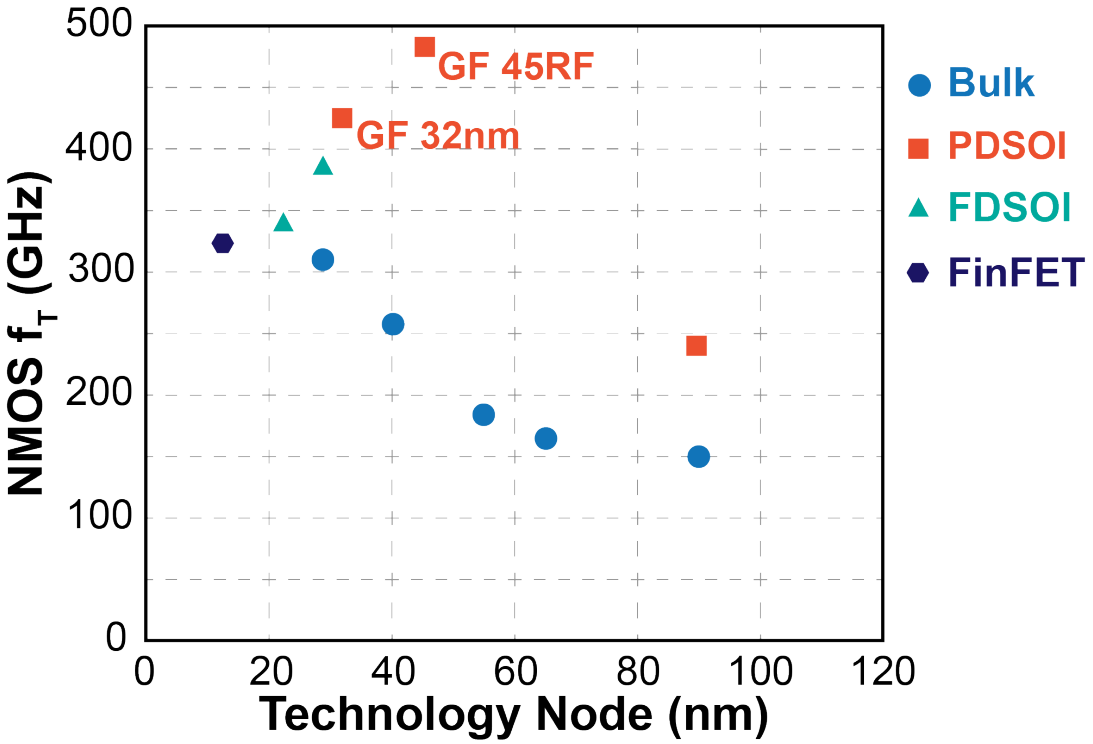

[Stojanovic, Opt. Ex 2018]

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You can hit end-game 100Gbps data rates!!

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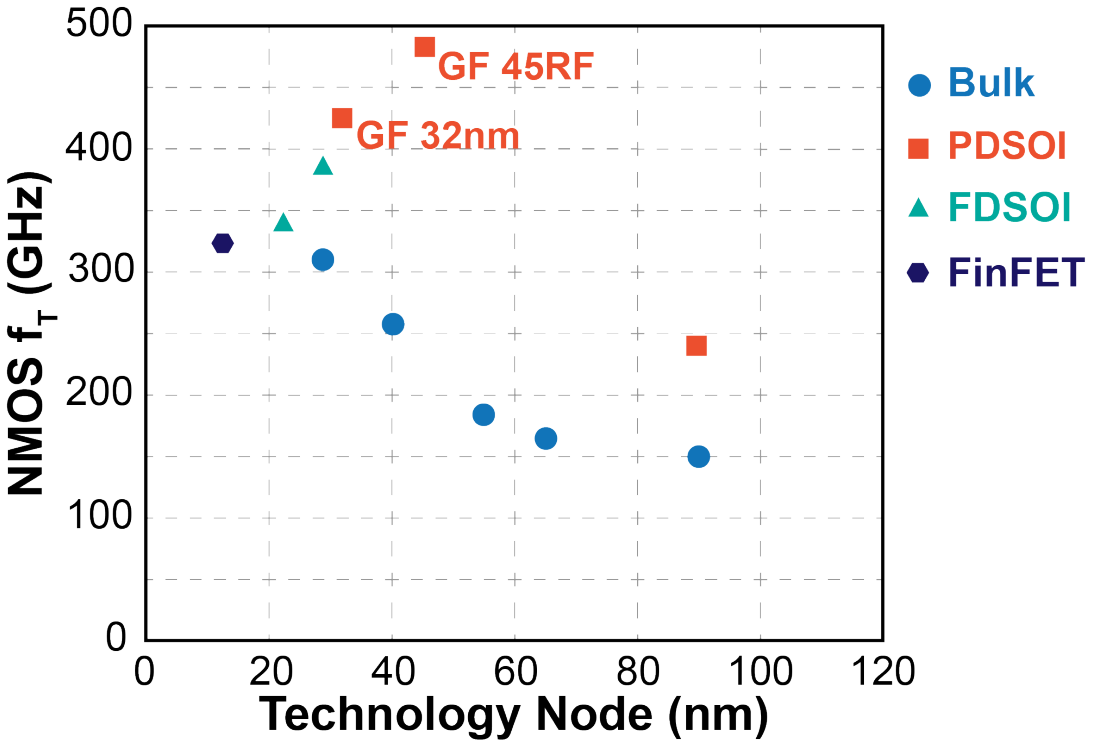

[Stojanovic, Opt. Ex 2018]

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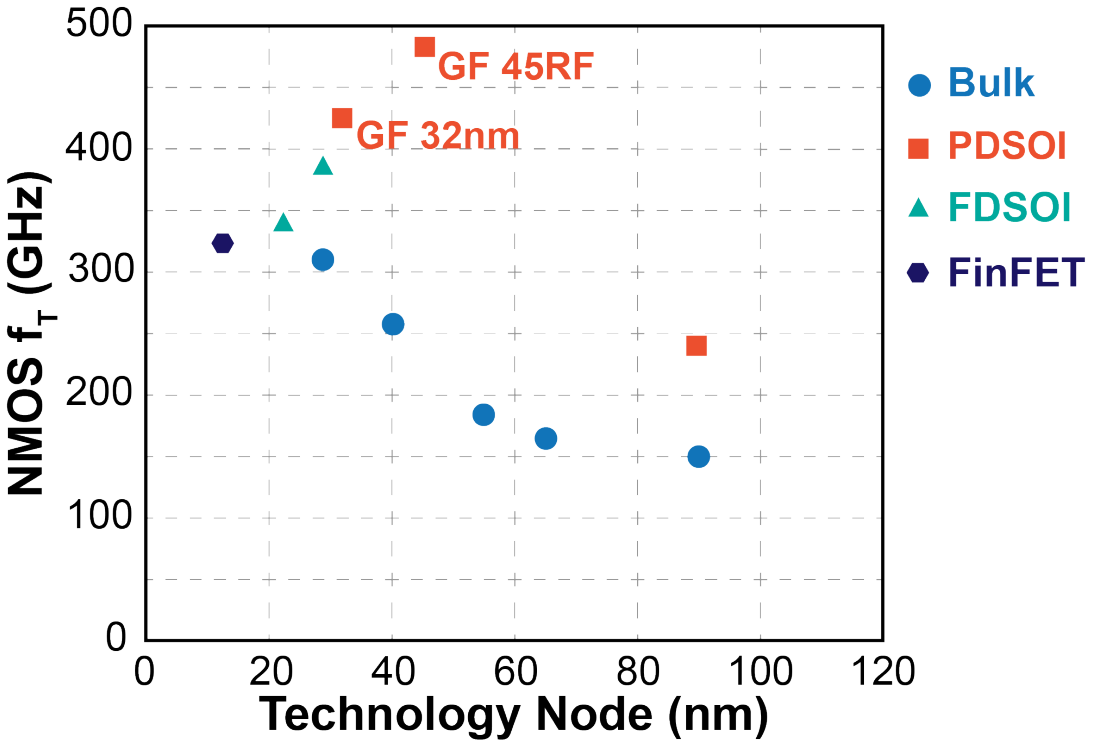

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- Transistor performance comparable or exceeding leading-edge nodes
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- Most advanced node before any double patterning needed or EUV

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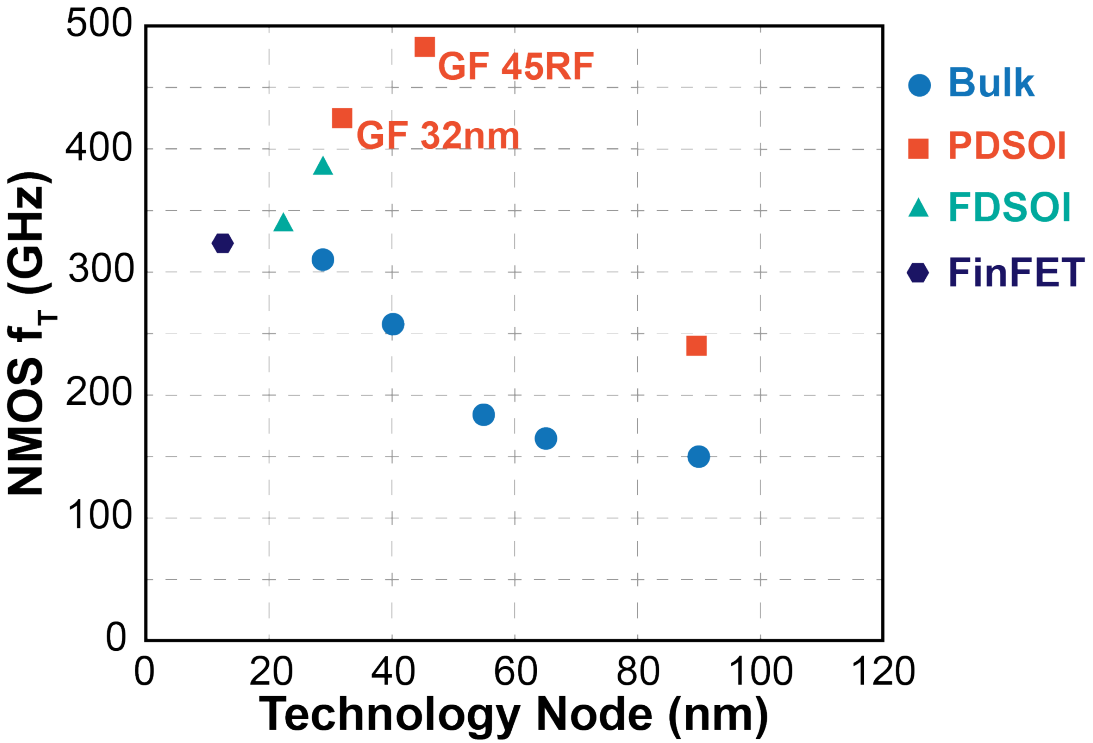

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- One of the last SOI nodes that support an optical mode natively in its c-Si transistor layer

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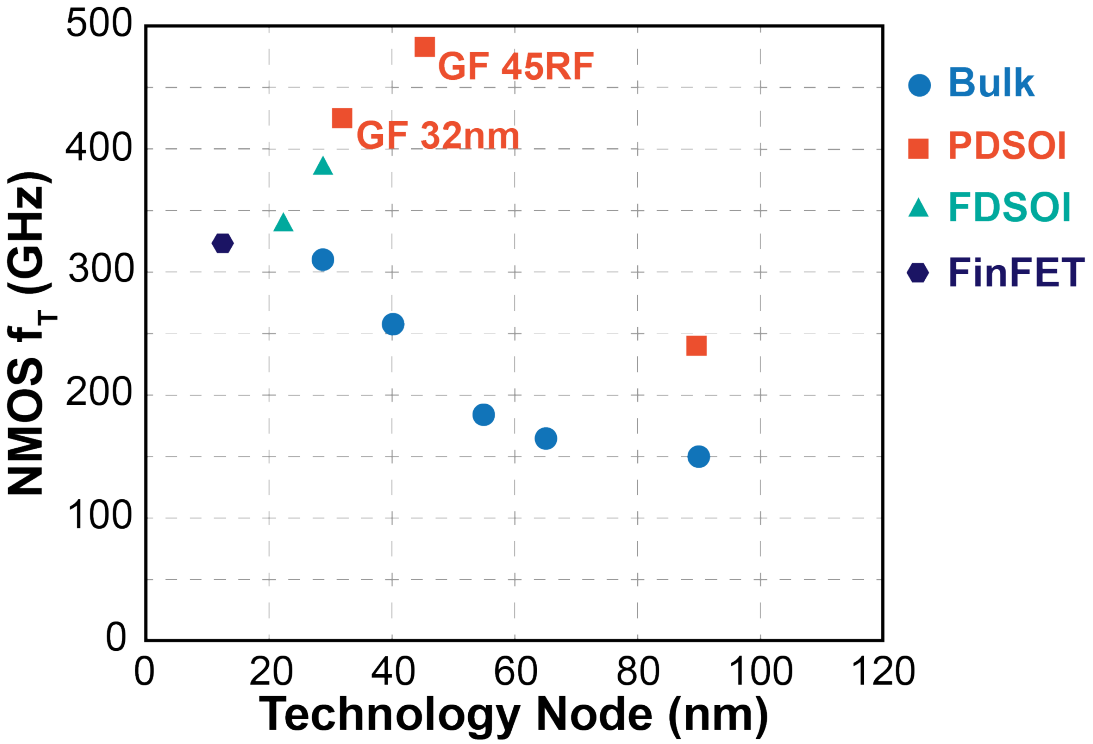

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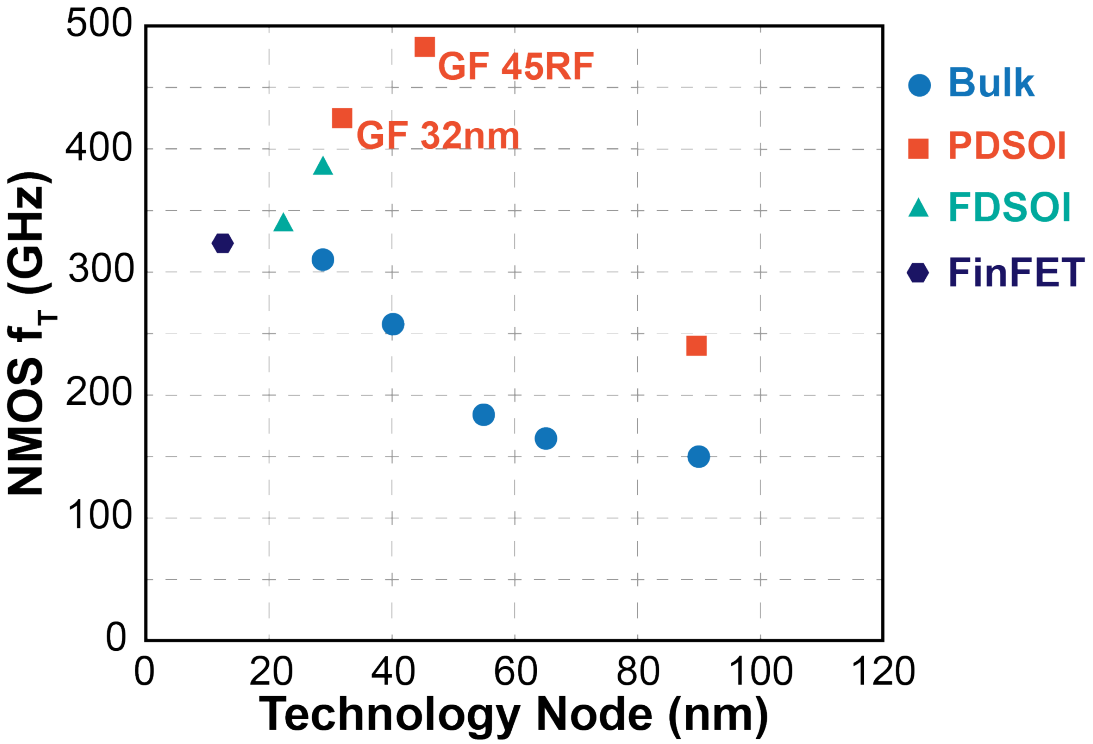

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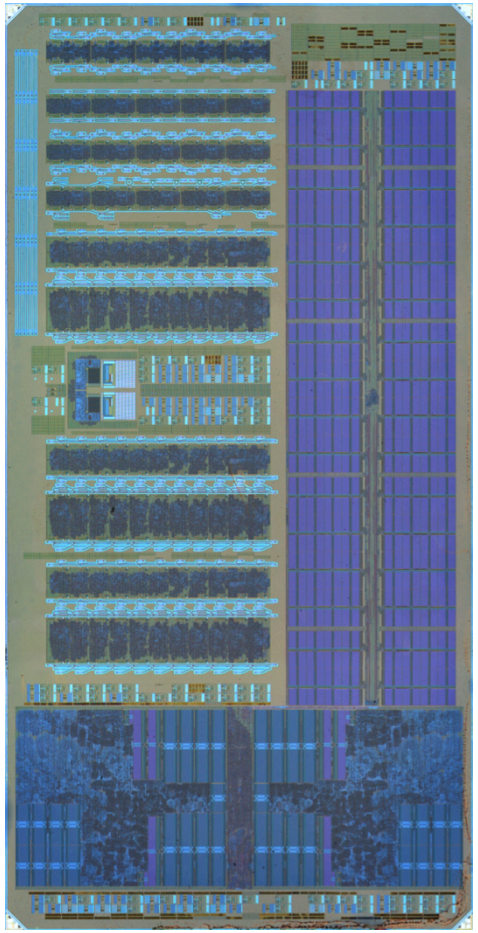
- Most advanced node before any double patterning needed or EUV
- One of the last SOI nodes that support an optical mode natively in its c-Si transistor layer
- SiGe present for transistor strain engineering
- An SOI CMOS node, qualified billion transistor designs

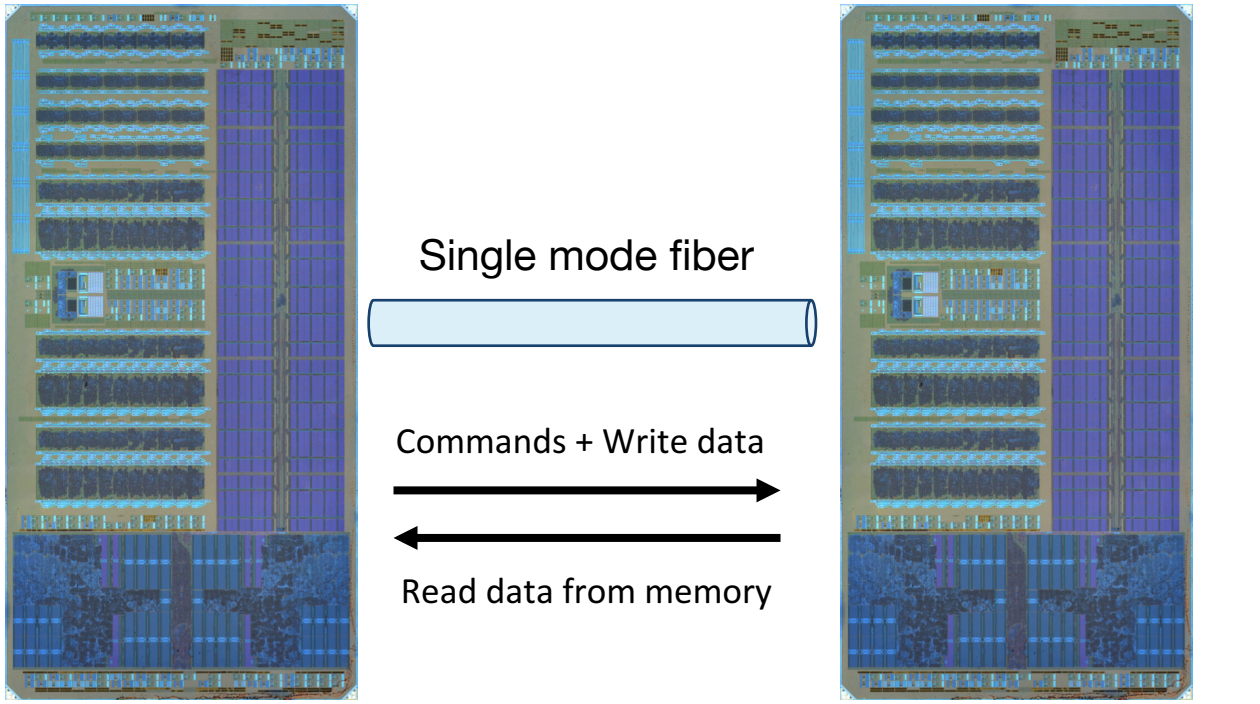
Single-chip microprocessor with photonic I/O



[Sun et al Nature 2015]

- Single chip with both electronics and optics
- 70M transistors alongside ~1,000 optical devices
- First microprocessor chip to communicate using light

Single-chip microprocessor with photonic I/O



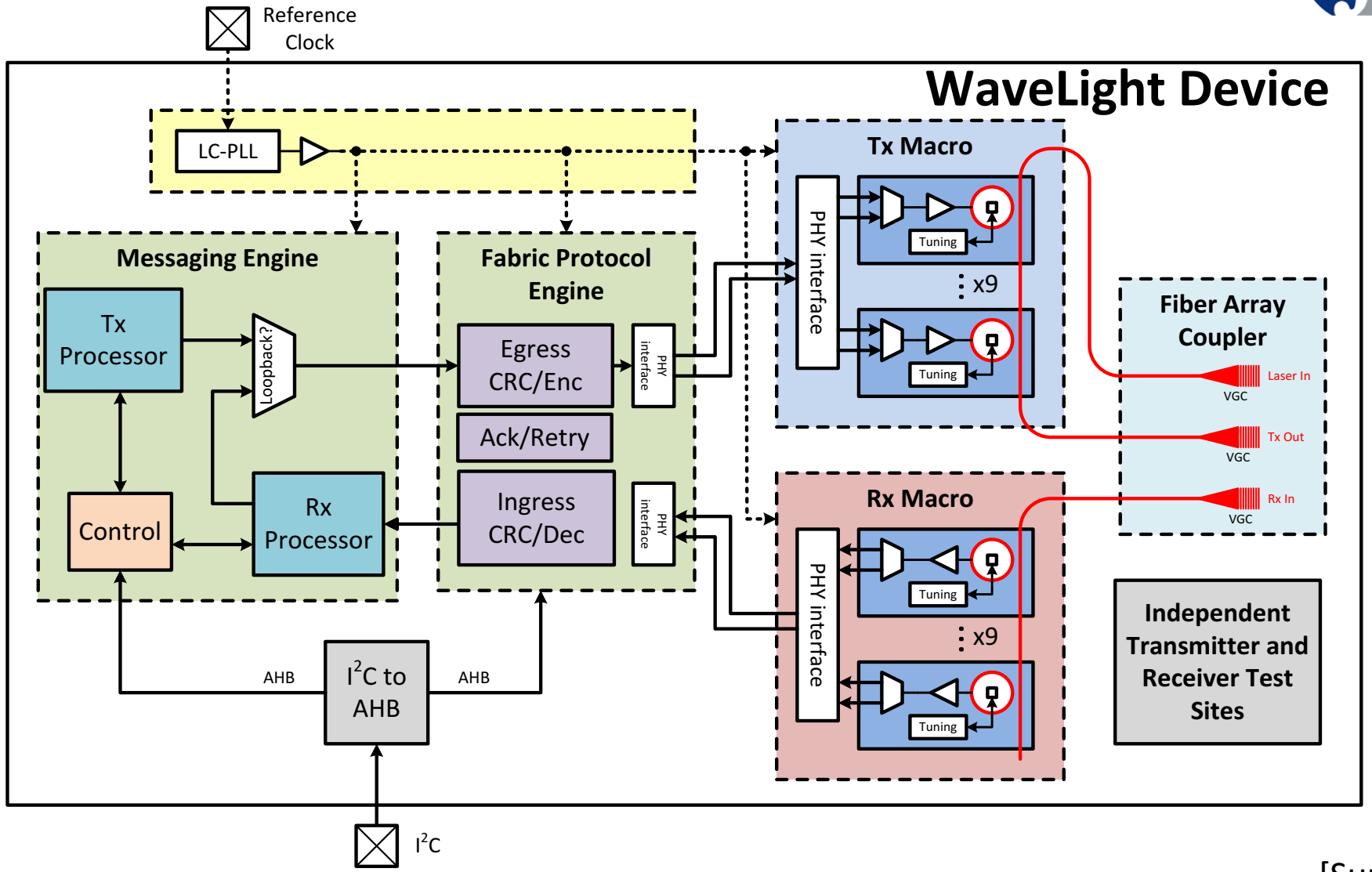
CPU mode

"DRAM" mode

- Dual-core RISC-V processors
- 1MB on-chip SRAM
- Two modes:
  - CPU mode
  - emulated DRAM mode
- Runs arbitrary compiled code
  - Linux
  - Graphics rendering
  - Performance benchmark tools

[Sun et al Nature 2015]

WaveLight: Low-latency switching fabric



[Sun *et al.* HOTI 2017]

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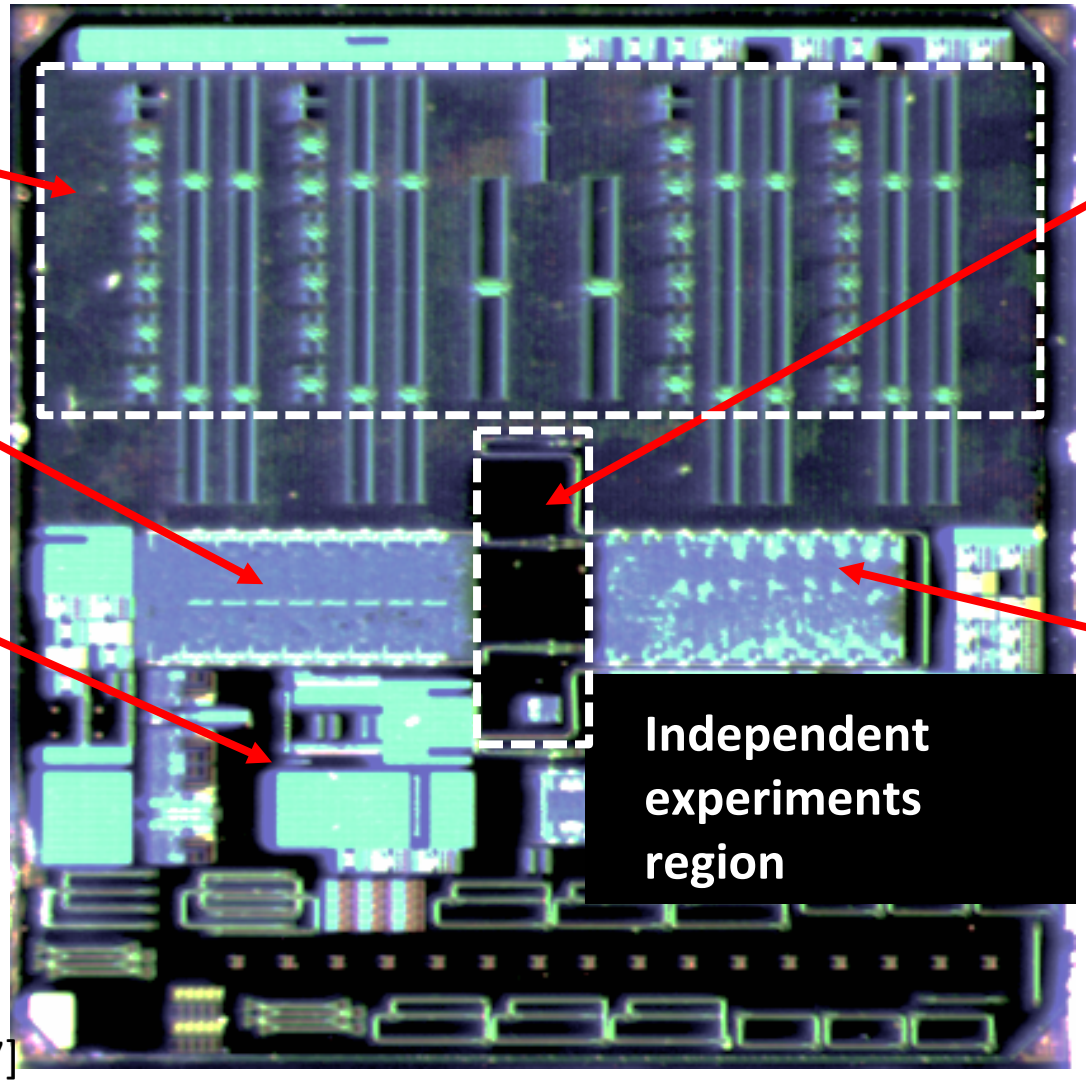
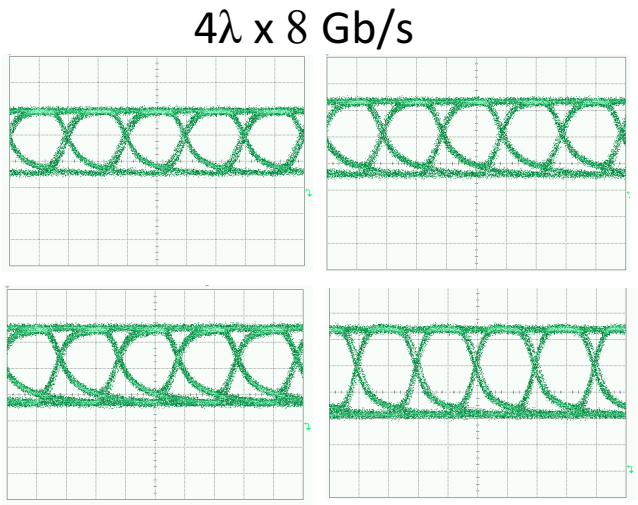
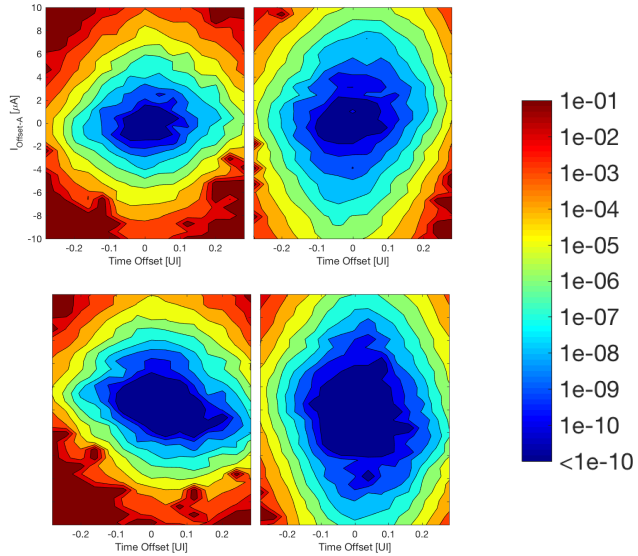
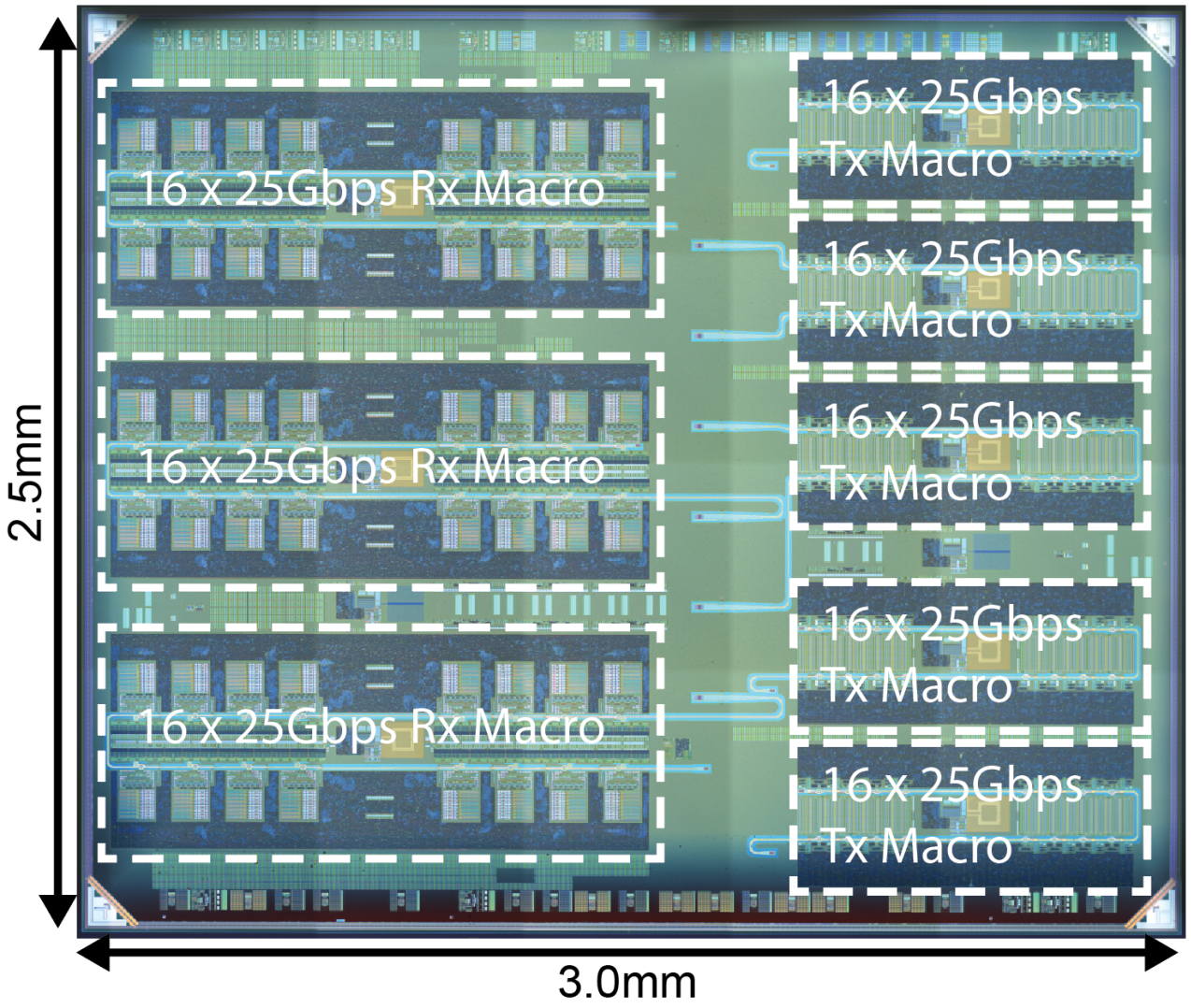




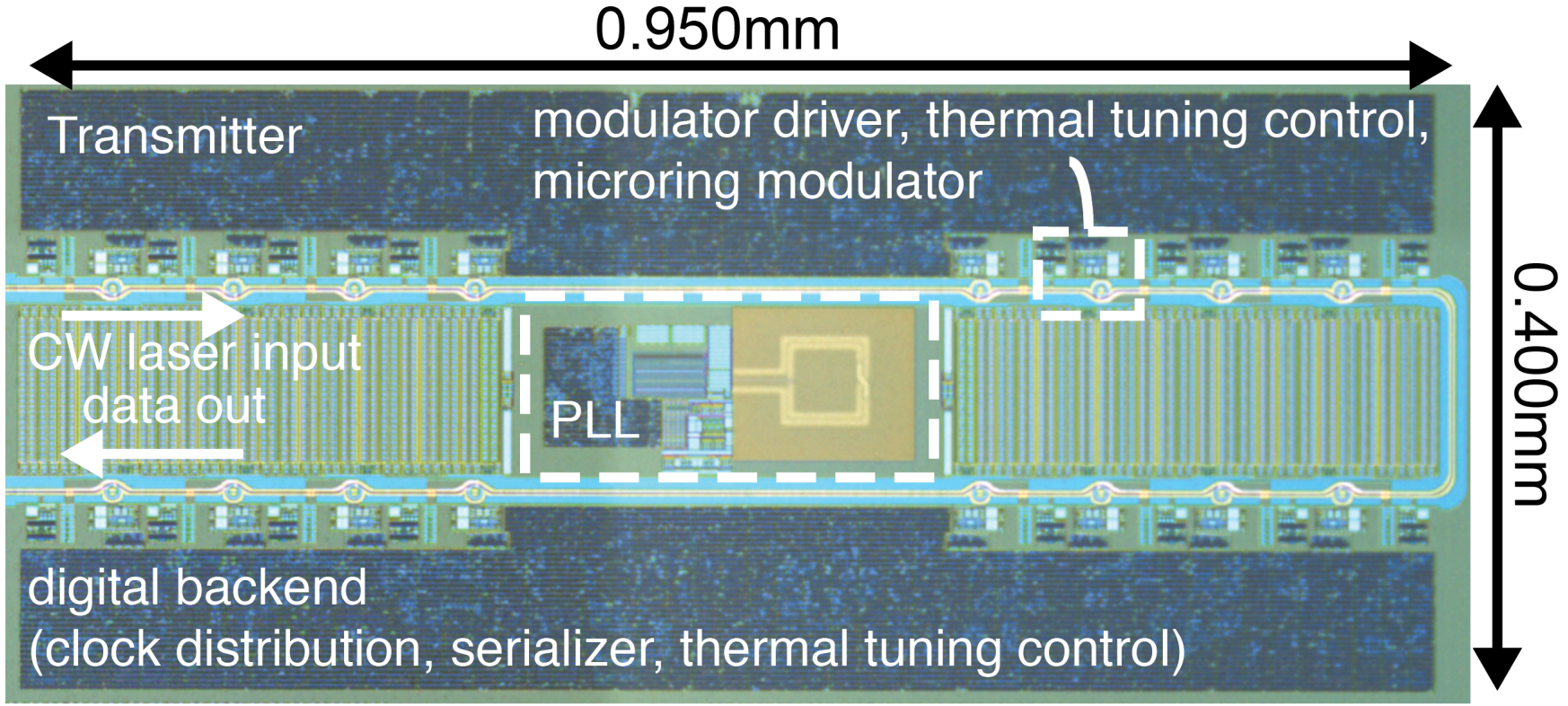


[Sun *et al.* HOTI 2017]

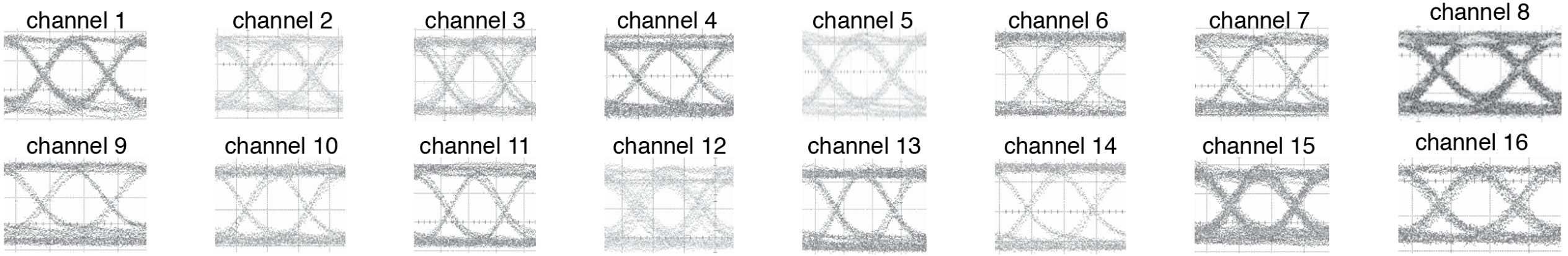
Monolithically integrated PICs for multi-Tbps I/O



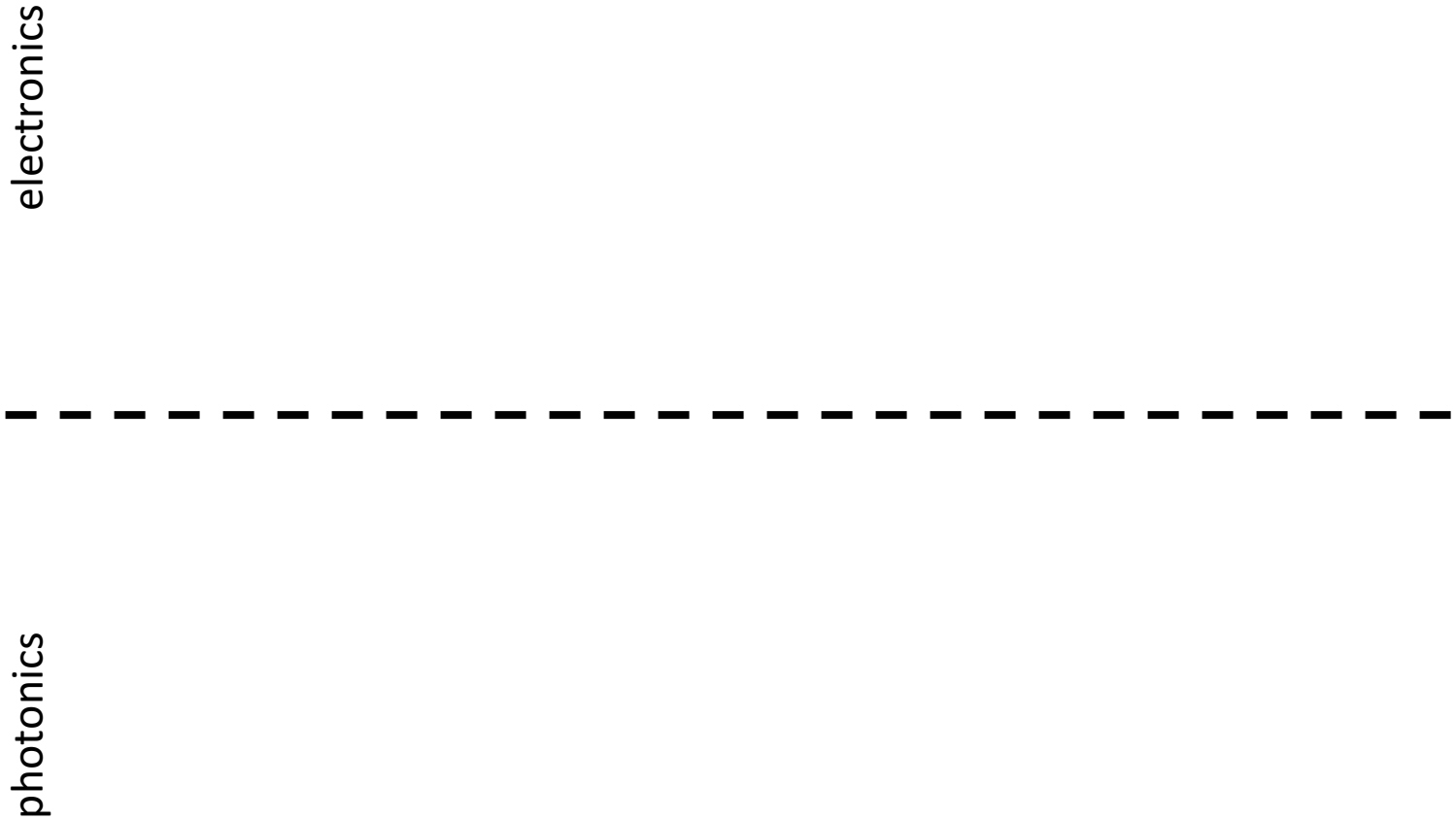
- Includes all electronics and photonics for optical I/O (except laser)
- Transmitter: 2.0 Tbps (5 x 400Gbps)
  - 16 x 25Gbps
  - Digital backend
  - SerDes
  - High-speed clocking, distribution
  - Closed-loop thermal control
  - Built-in self test (BERT, debug, etc.)
- Receiver: 1.2 Tbps (3 x 400Gbps)
  - 16 x 25Gbps
  - Digital backend
  - SerDes
  - PD, TIA, equalization, CDR, clocking



- 400G Tx
- ~1 Tbps/mm^2
- 0.83 pJ/bit



Design flow



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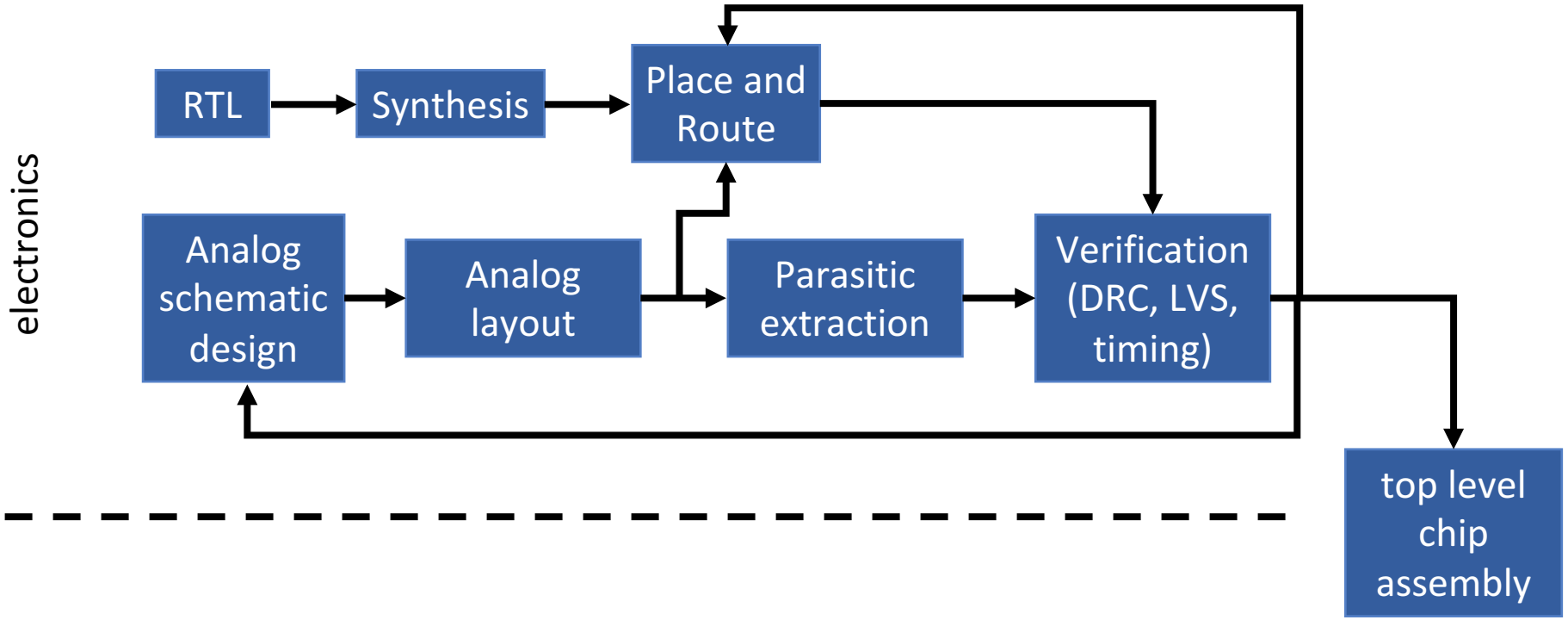

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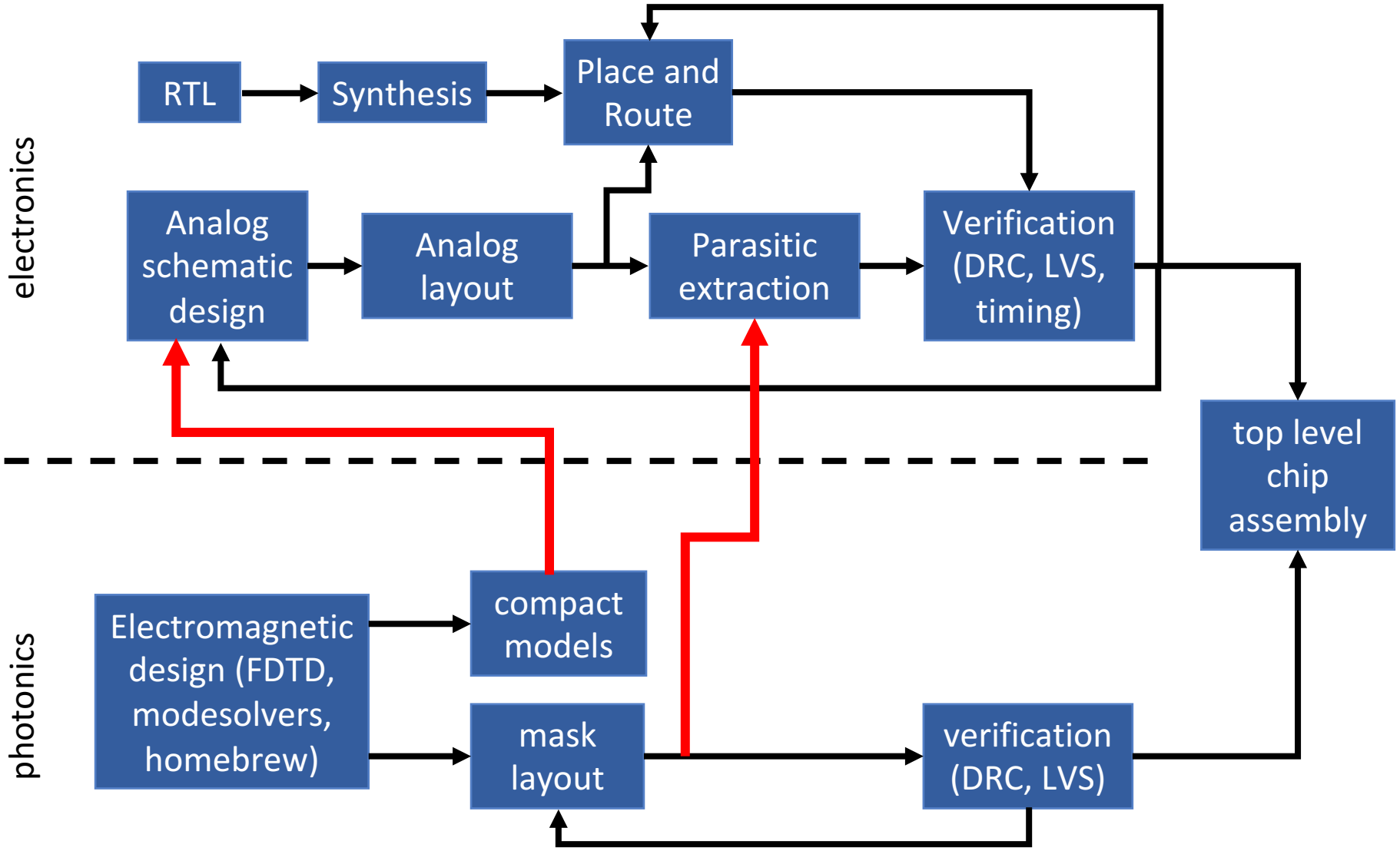

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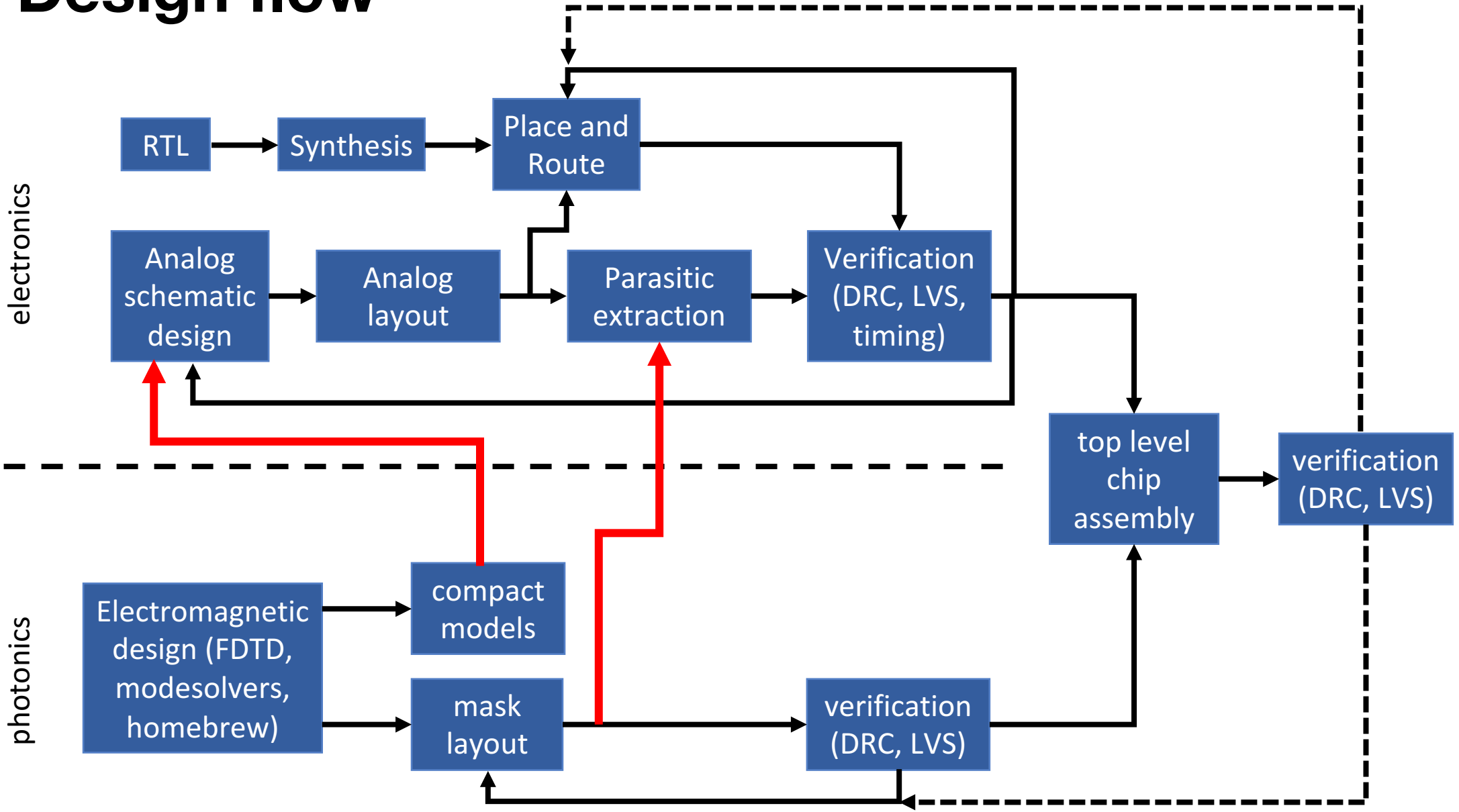

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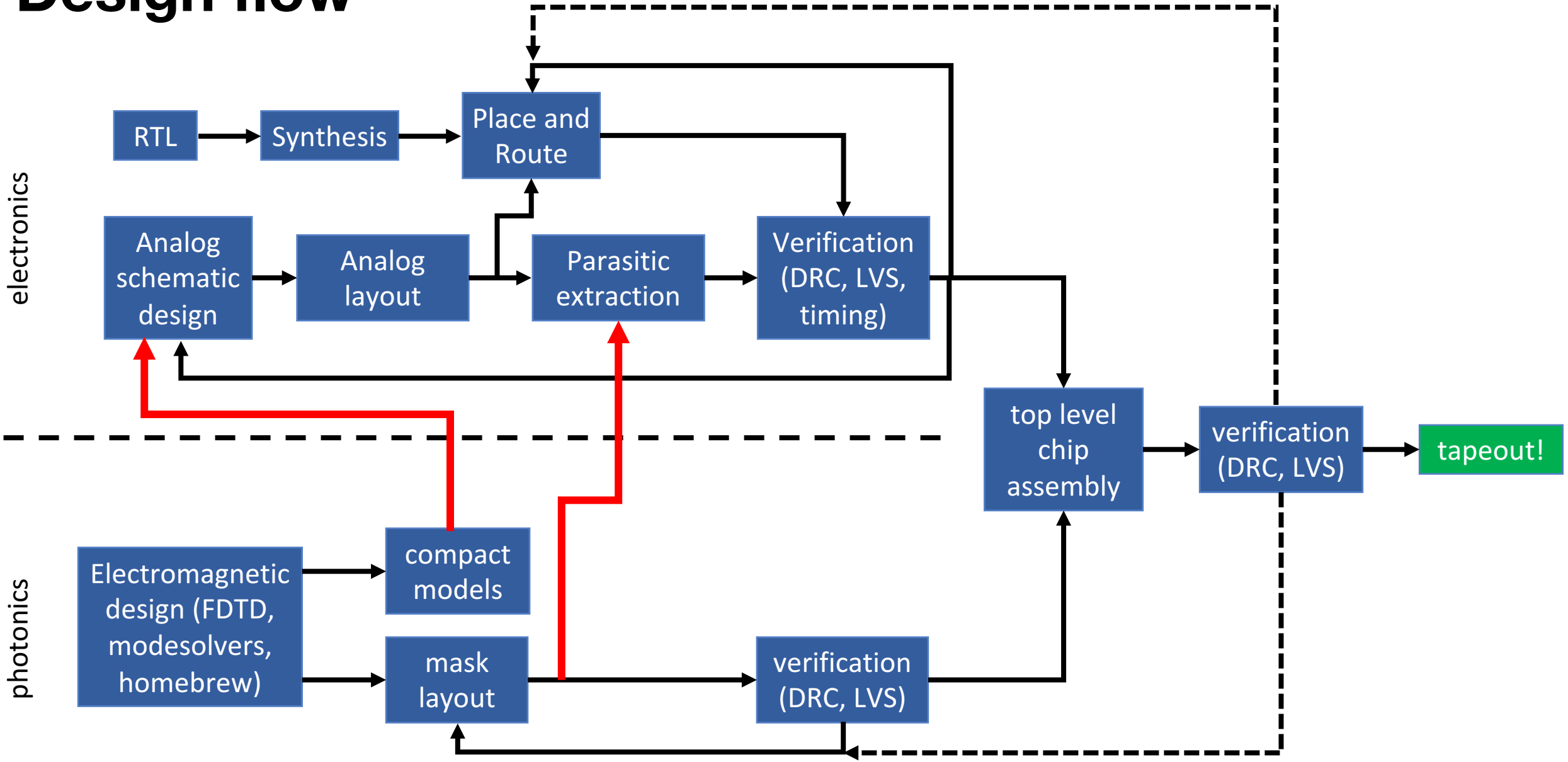
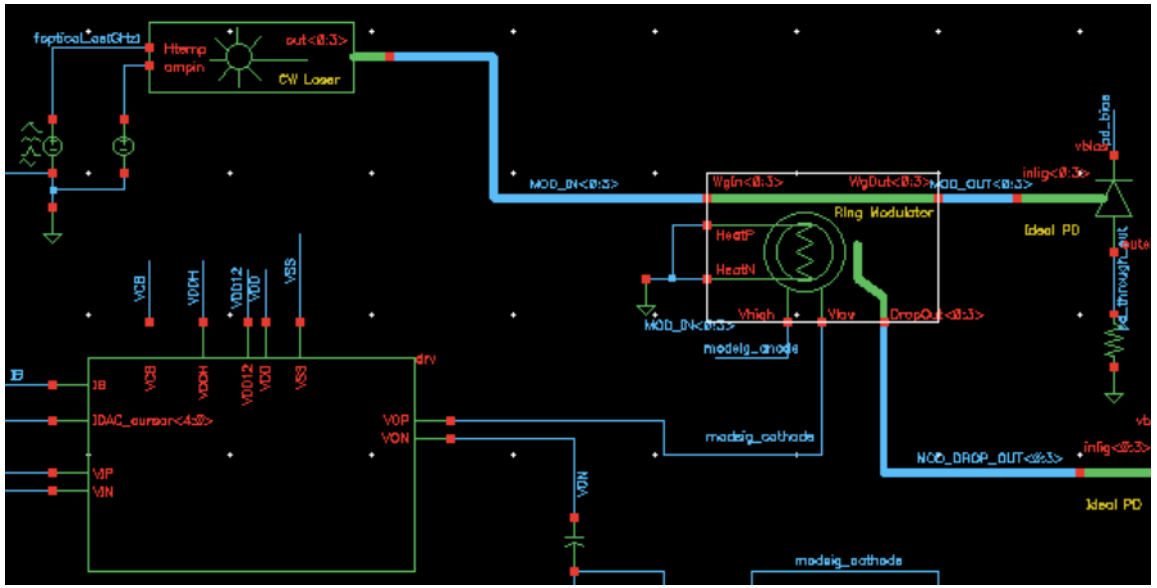
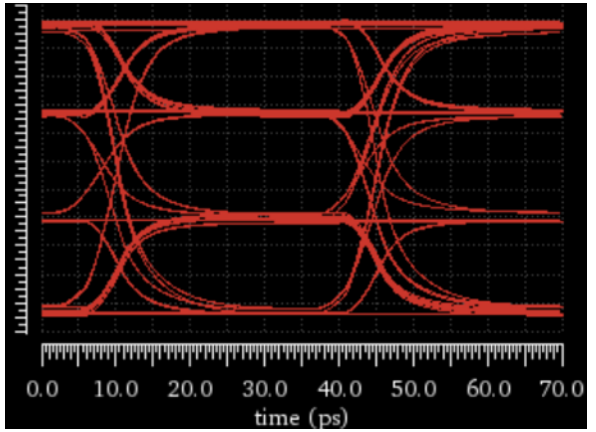


Co-design simulation environment

- Device simulations for compact model parameter extraction
  - Lumerical FDTD, Mode, Device
  - COMSOL
- Verilog-A device compact models to integrate into electronic-photonic circuit simulations
  - Fully-dynamic models, not just base-band models
- Simulation done using established circuit simulation tools
  - Spectre/HSPICE
  - Run in the same simulation as with 45nm transistors

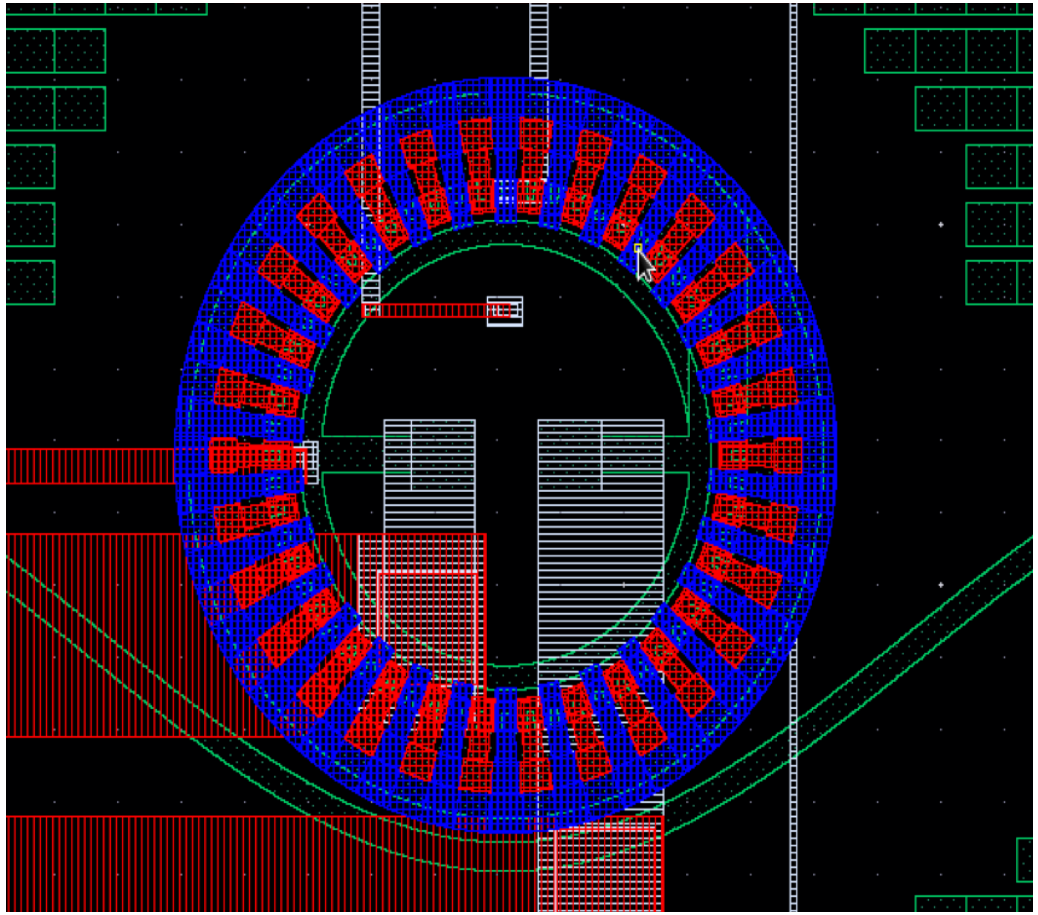




56Gbps PAM4

Parasitic extraction

- Connections between circuits and photonic devices using existing PDK metal layers
- Parasitic extraction deck will extract full signal path between circuits and optics
- Short wire lengths, parasitics are on the order of 1-2fF
- Extracted netlist plugs directly into simulation framework

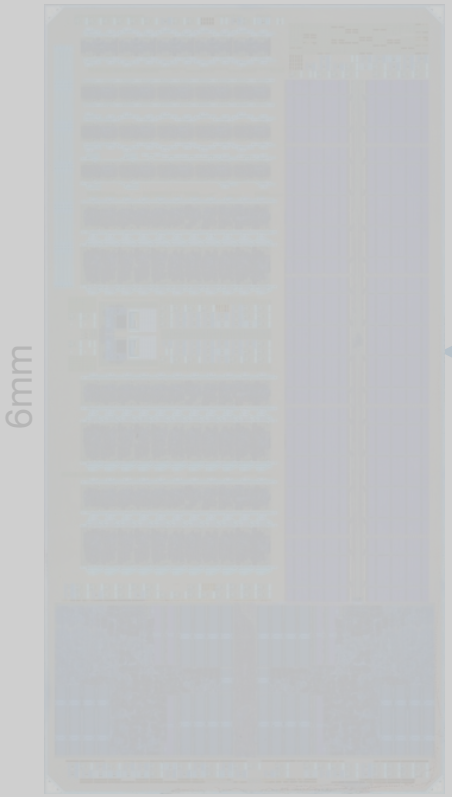


Outline

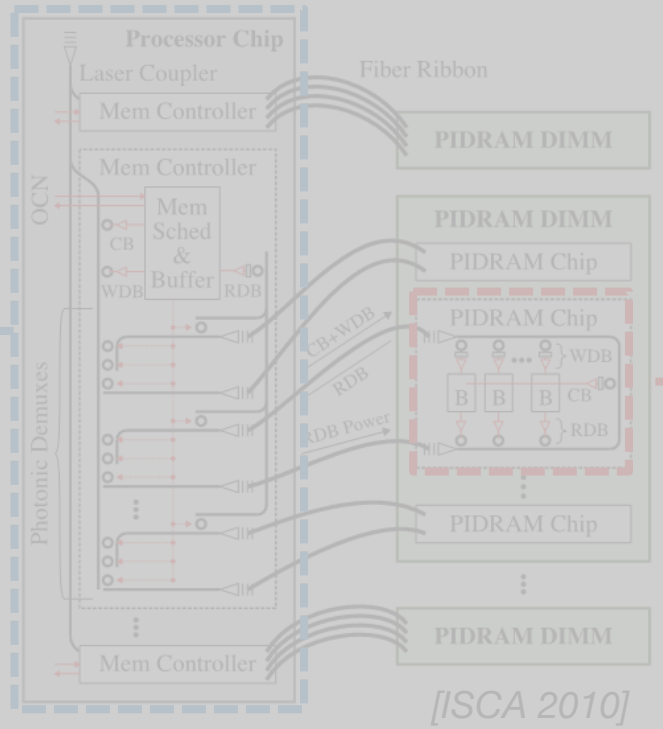
- Introduction and motivation
- Photonics in SOI CMOS
- **Photonics in Bulk CMOS**

Photonic processor to memory interconnect

High Performance 45nm SOI



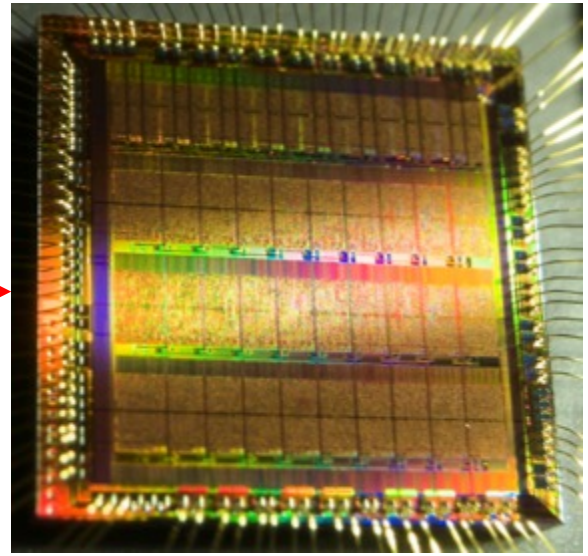
70M transistors
1000 optical devices



[ISCA 2010]

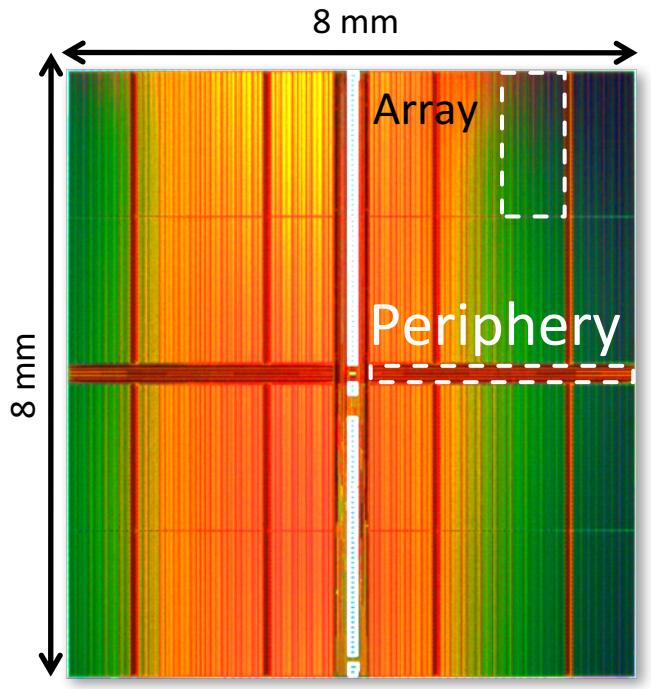
DARPA POEM

0.180µm Bulk

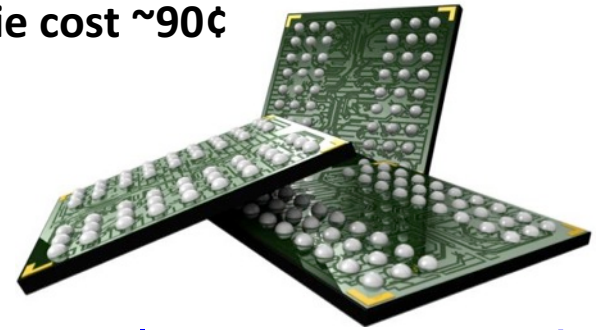


2M transistors
1000s optical devices

DRAM processes heavily optimized for cost

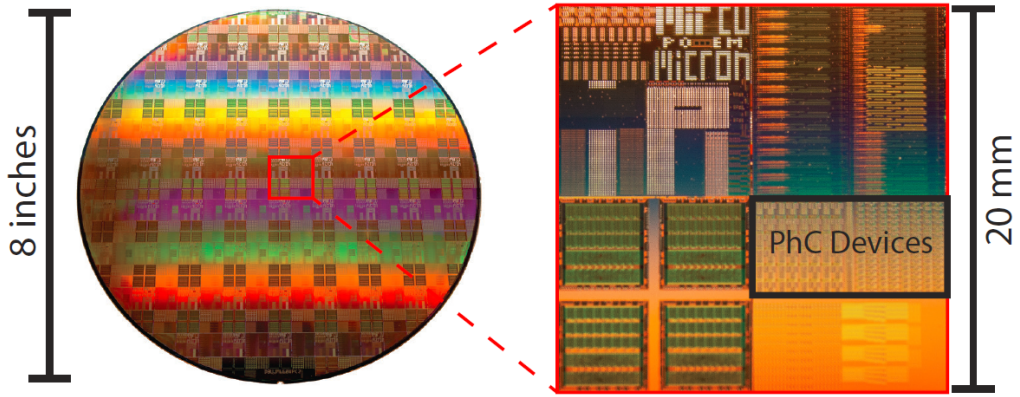


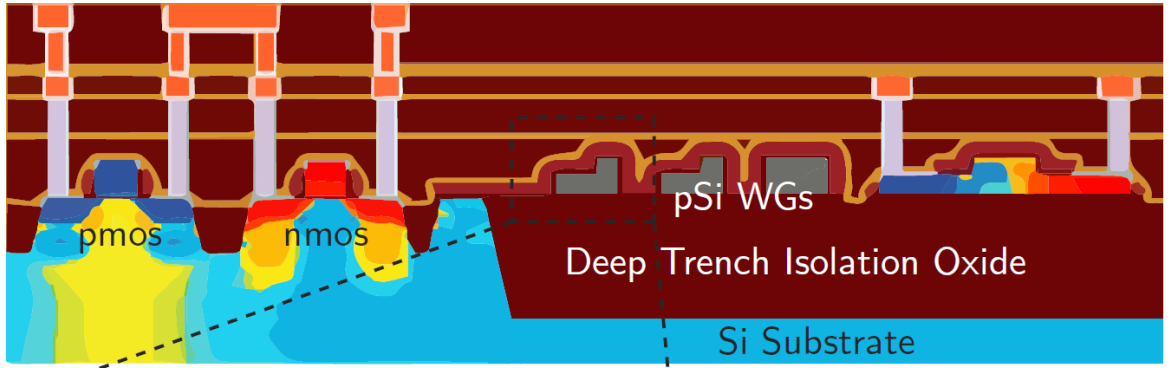
DDR3-1333 Technology
2 Gb die cost ~90¢

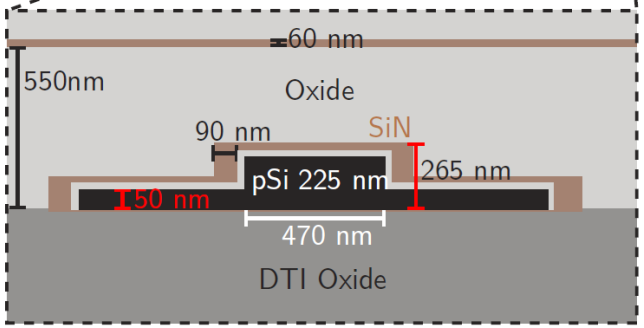


Meade et al. OI 13, VLSI Tech Symp 14

Micron wafers





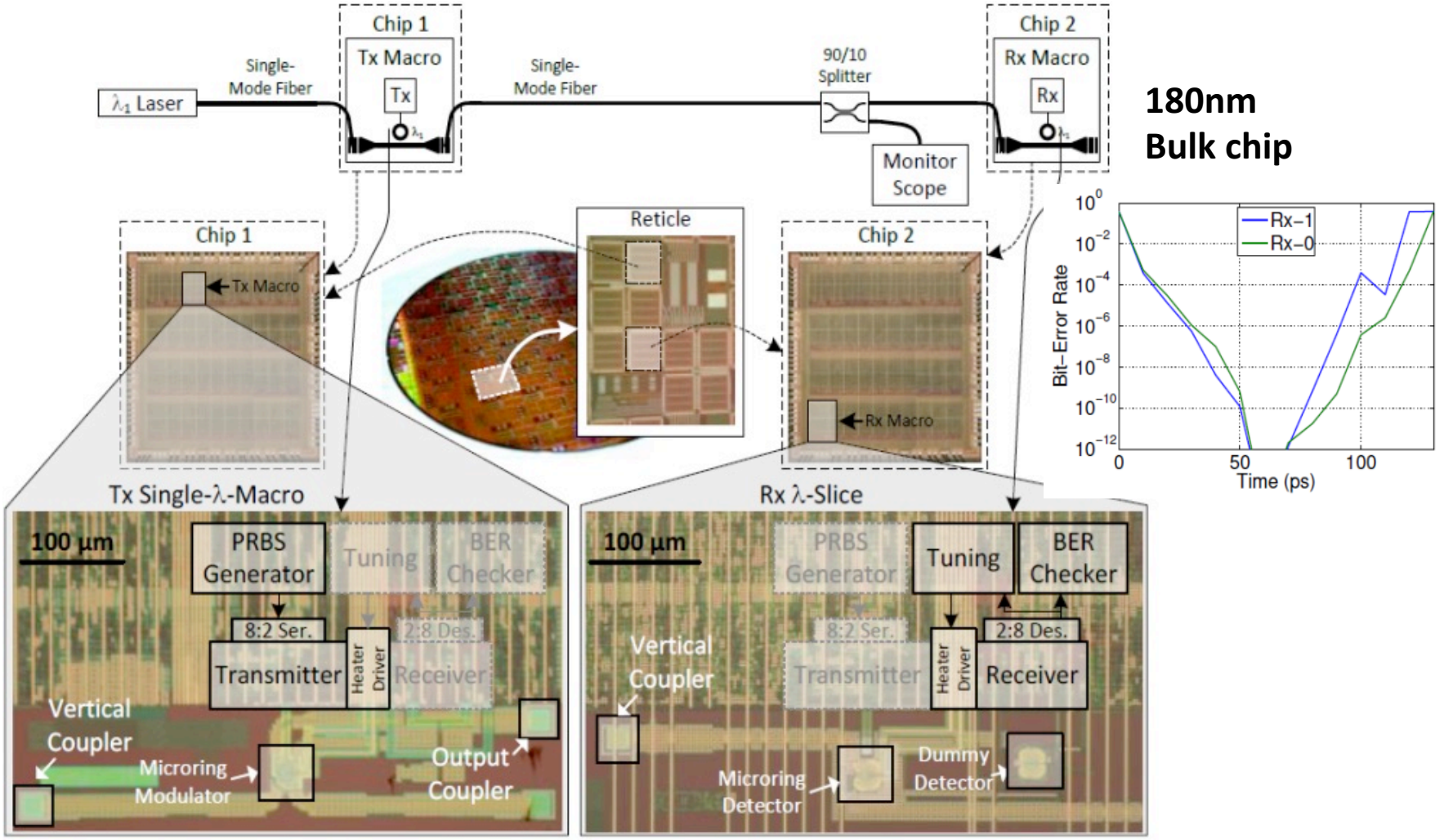


Key constraints:

- Bulk Substrate
- Low Cost
- No SiGe

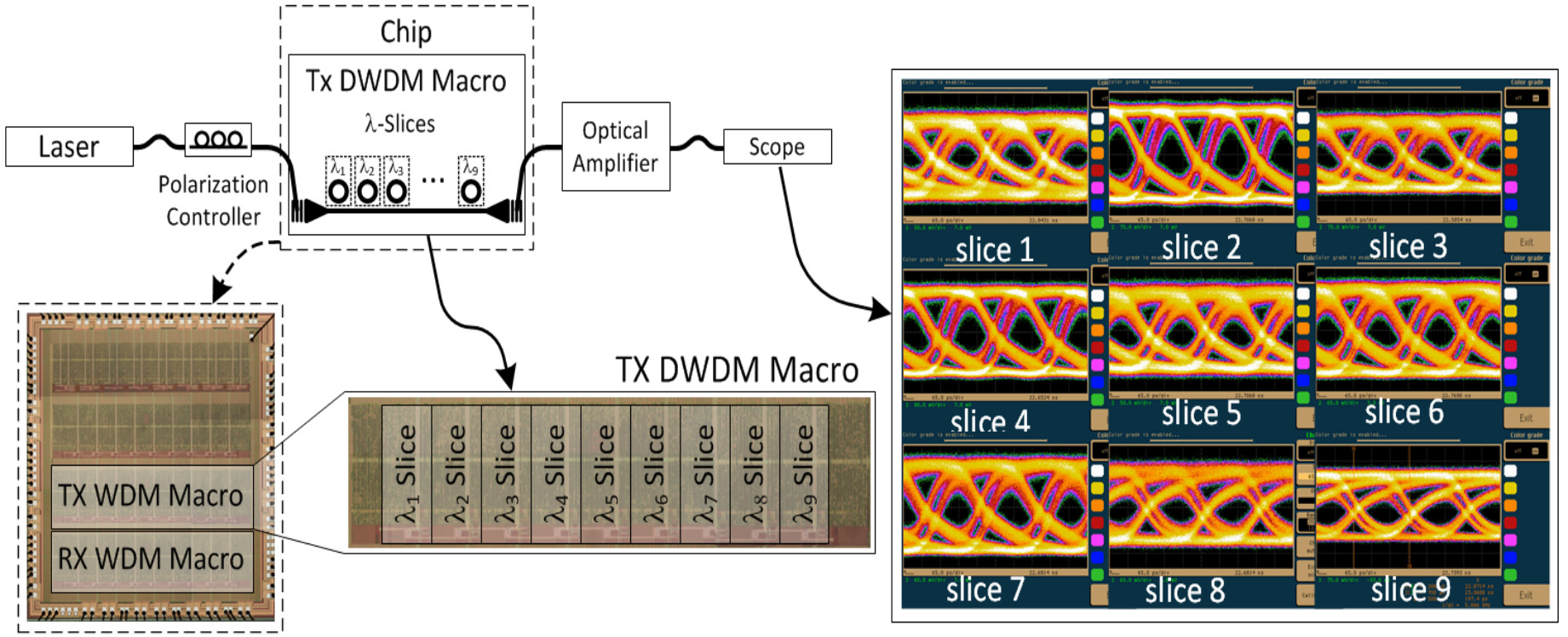
First-ever link result with bulk CMOS photonics

Micron D1L Reticle

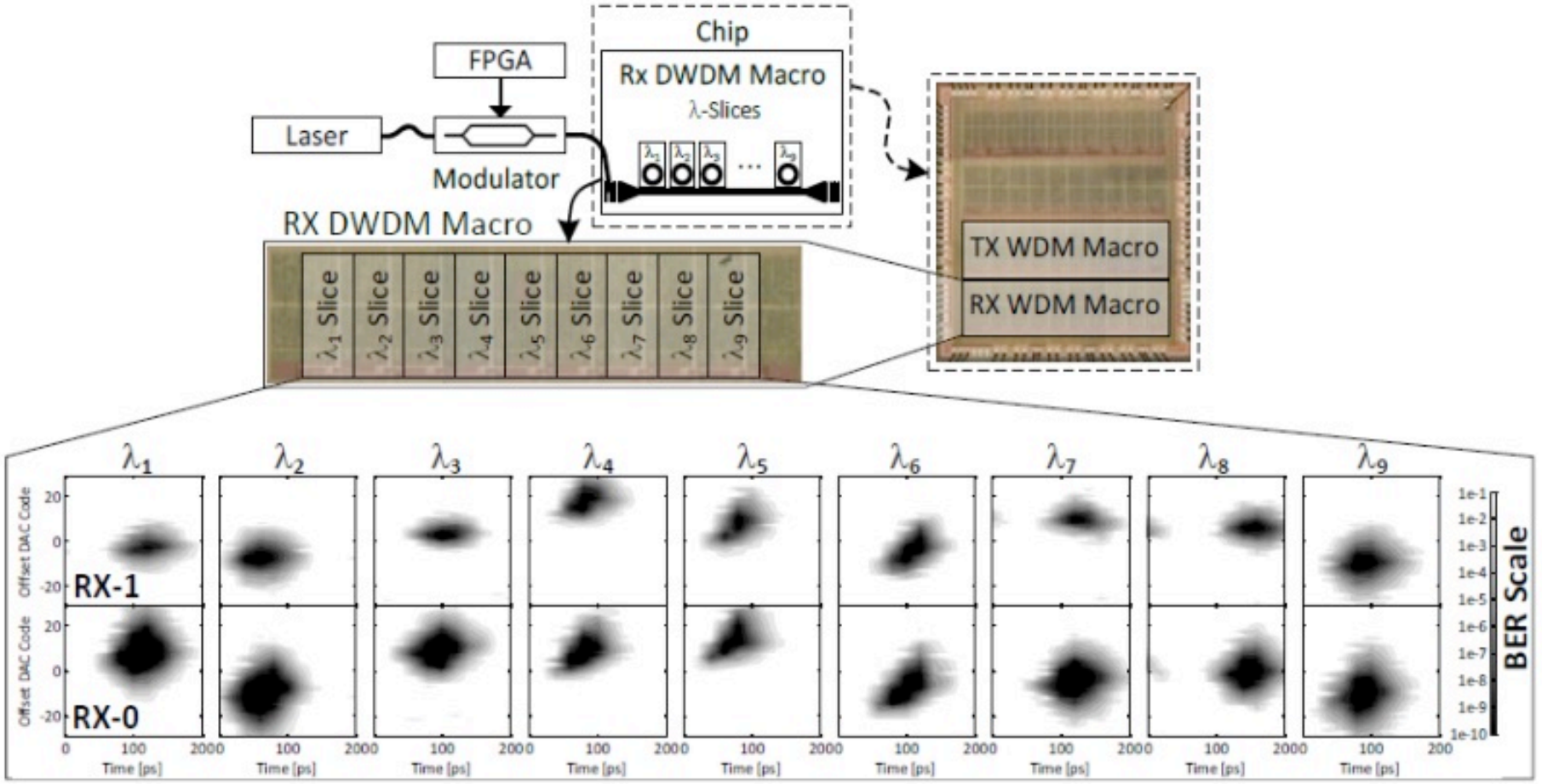


180nm
Bulk chip

[Meade et al. VLSI Tech Symp 14, Sun et al VLSI Ckts Symp 14]



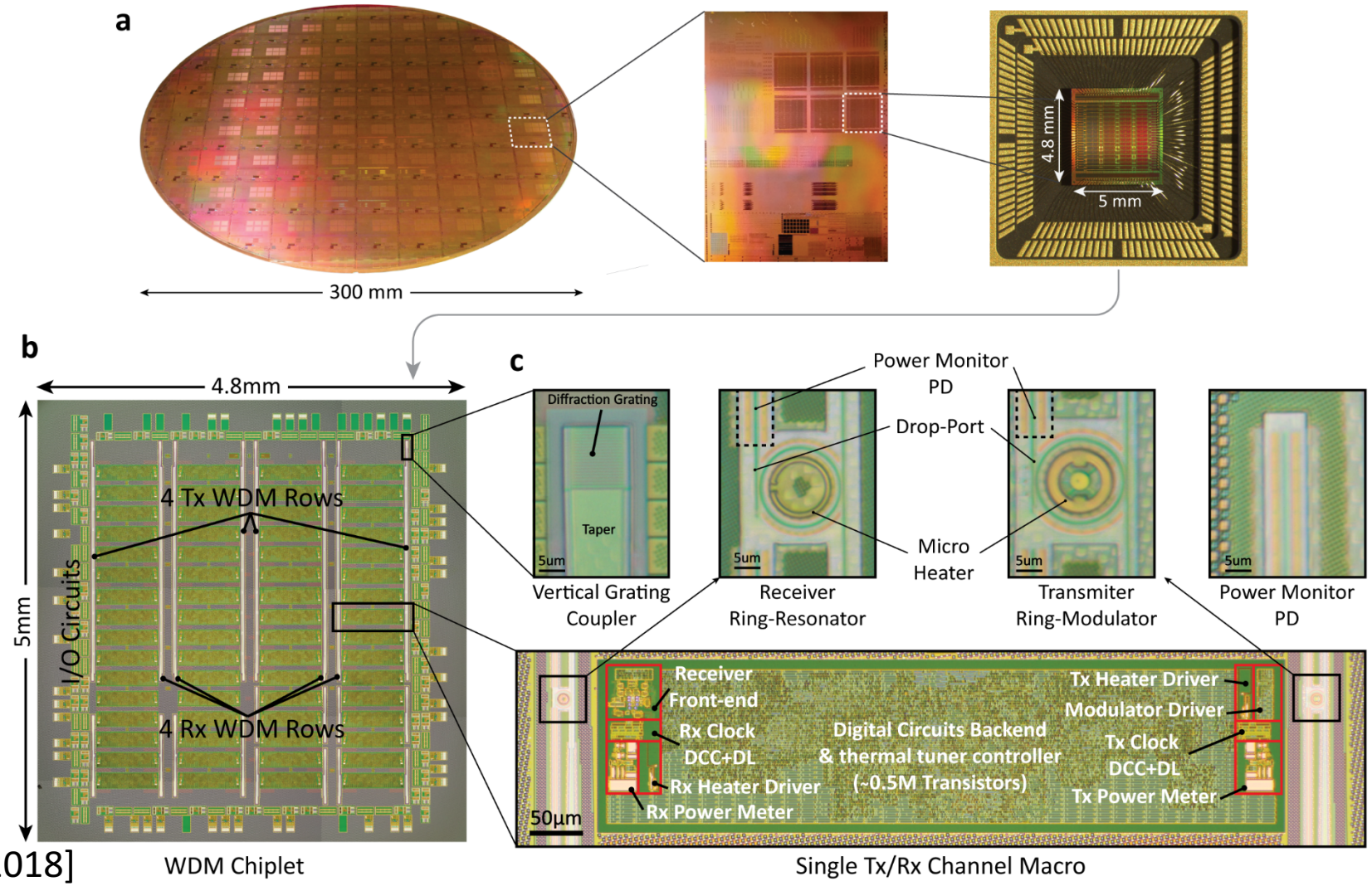
- All slices BER checked at 5Gb/s
- 45Gb/s aggregate rate per waveguide



- All receive slices functional and BER checked at 5Gb/s
- Single fiber more I/O BW than x16 DDR4 part

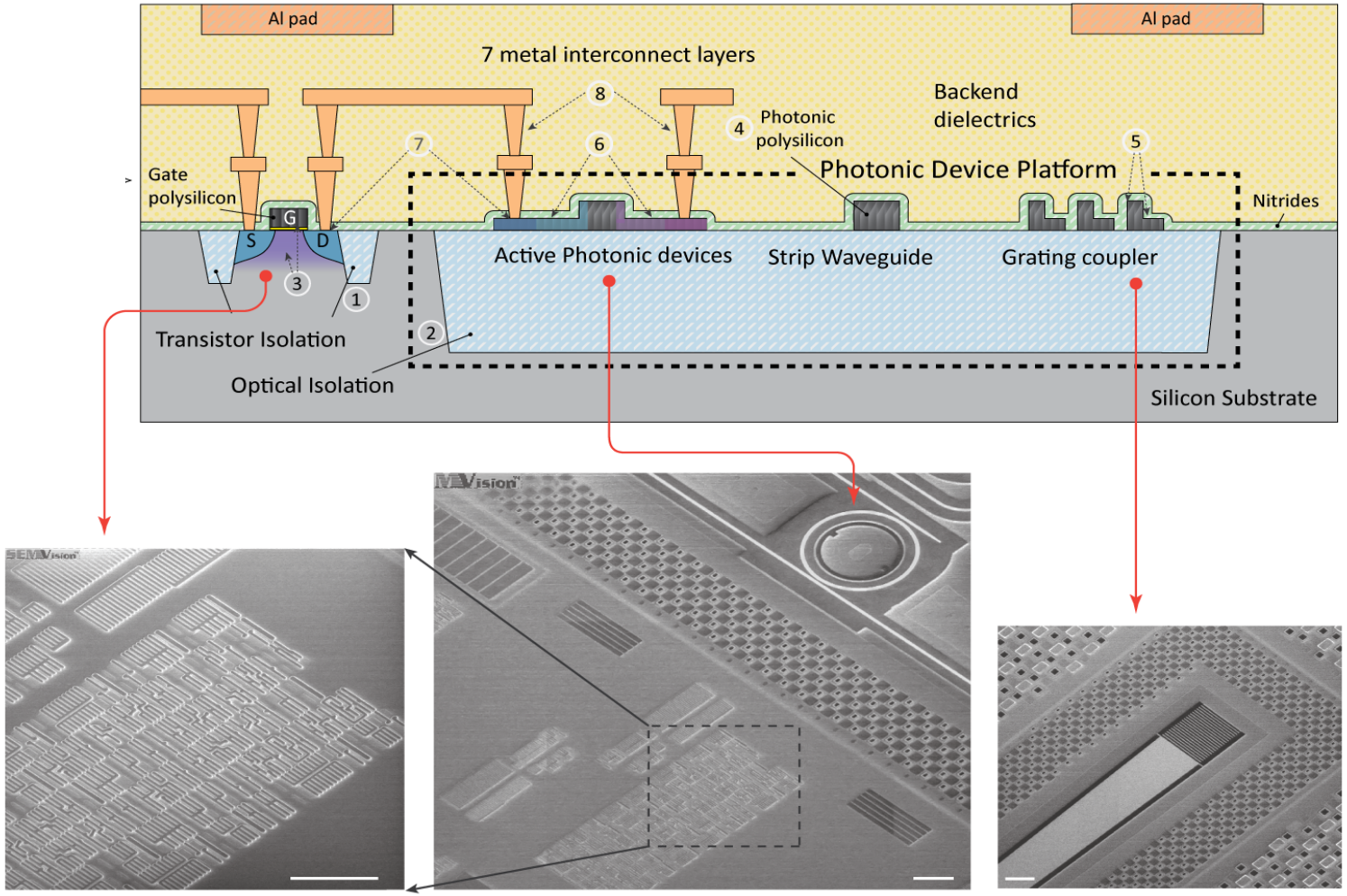
From 200mm to 300mm bulk CMOS

First 65nm bulk CMOS wafers with working photonics and transistors!



[Atabaki *et al.* Nature 2018]

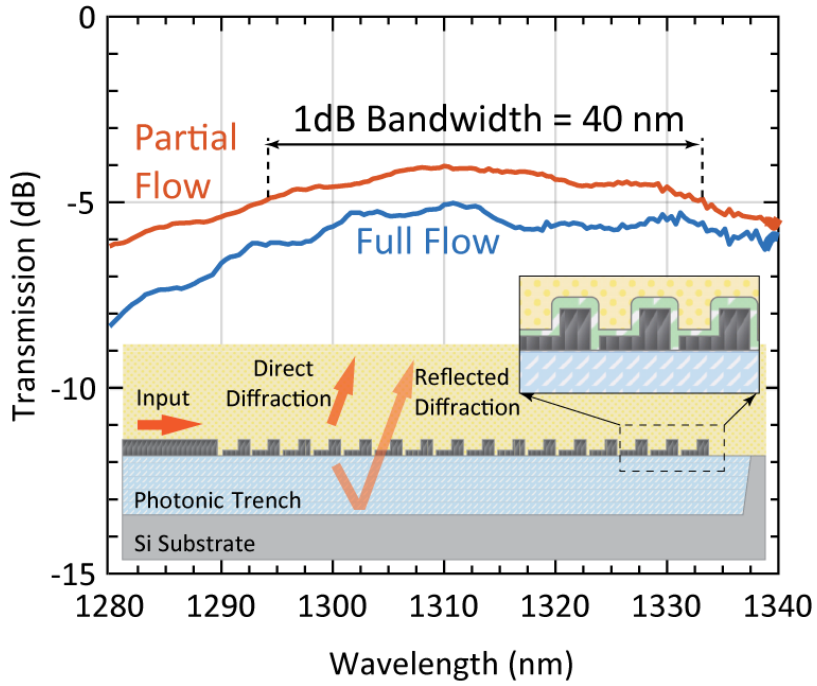
Process Integration

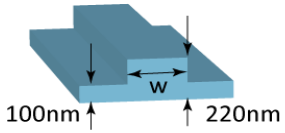
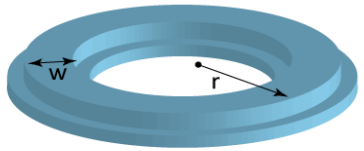
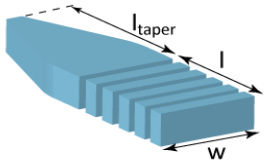


- Deposited on deep-trench oxide
- Patterned after transistor formation

[Atabaki *et al.* Nature 2018]

Device Library

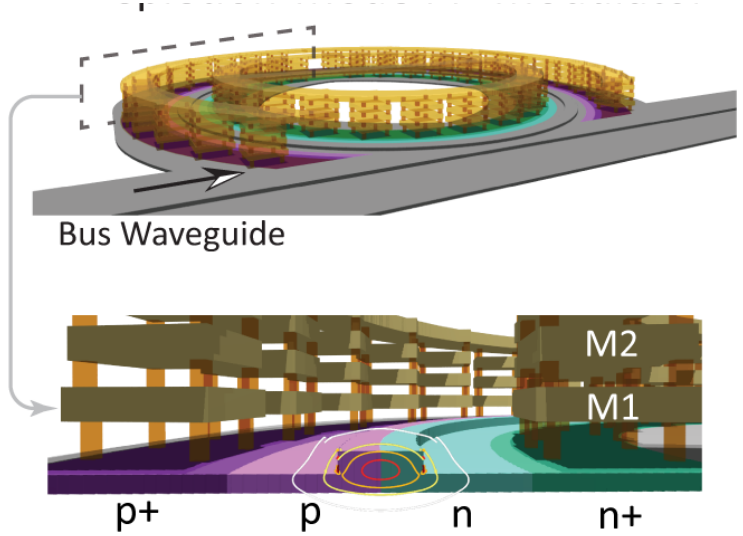


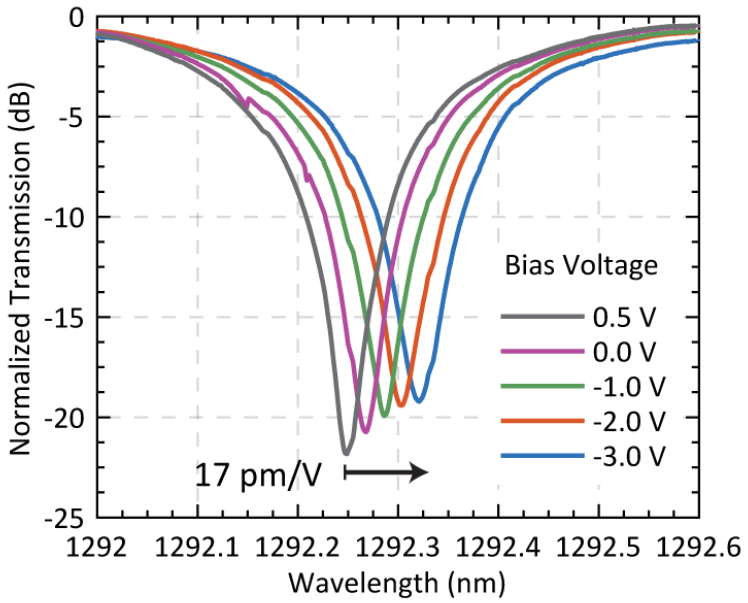
Ridge Waveguide	Ridge Microring	Grating coupler
		

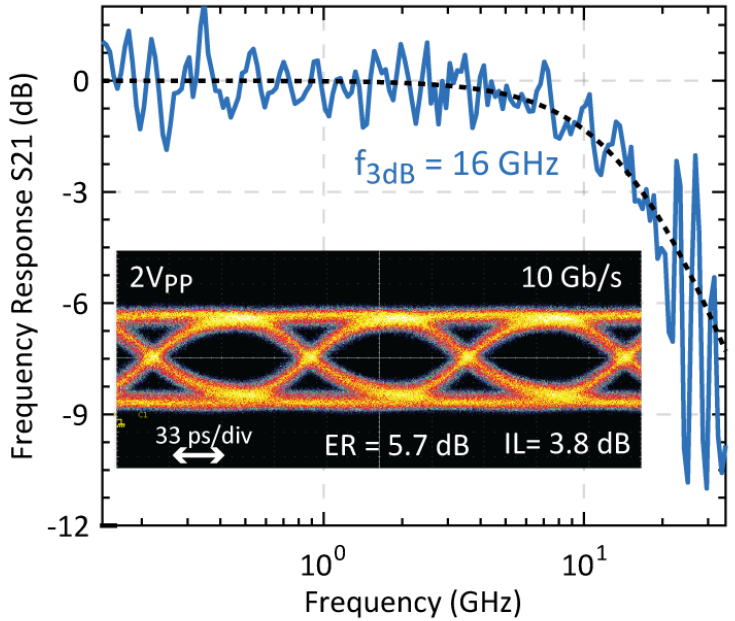
	Propagation Loss	Intrinsic Q	Coupling Loss
Partial Flow	8-15 dB/cm	19-31k	4.2 dB
Full Flow	21-27 dB/cm	10-19k	5.2 dB
Dimensions	w= 400 nm	w = 400 nm r = 7.5 µm	w = l = 8 µm l_{taper}= 250 µm

[Atabaki *et al.* Nature 2018]

Microring modulators

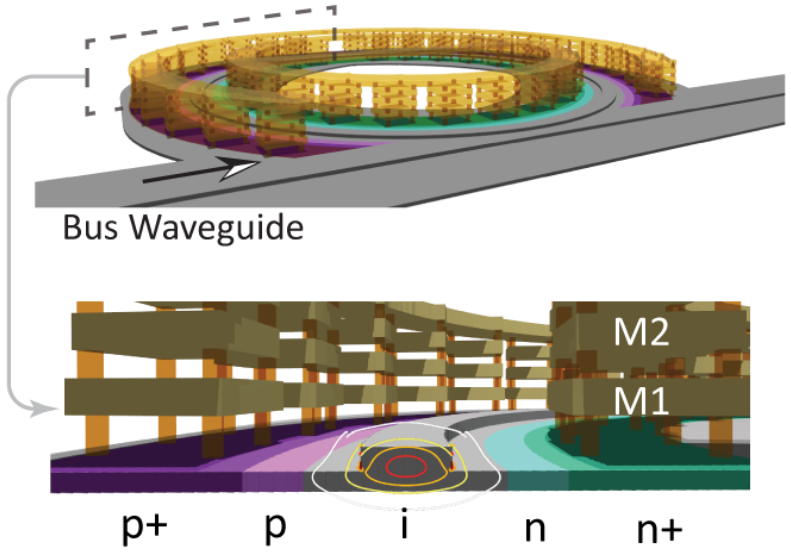


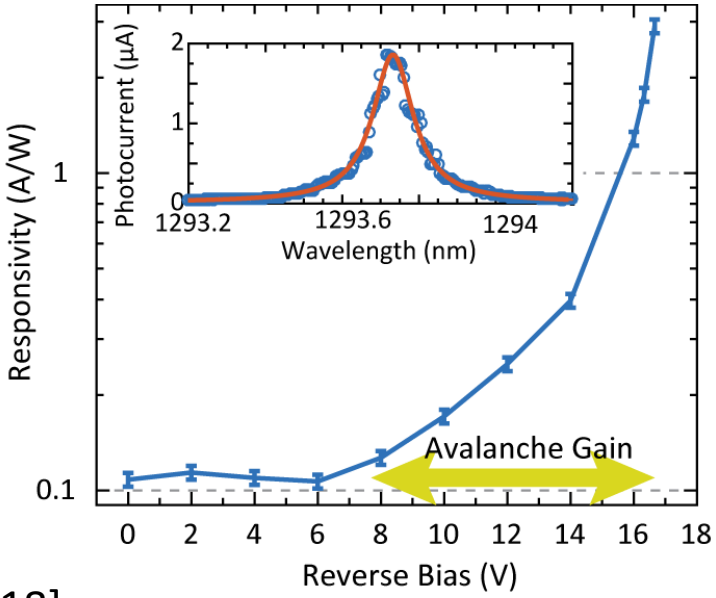


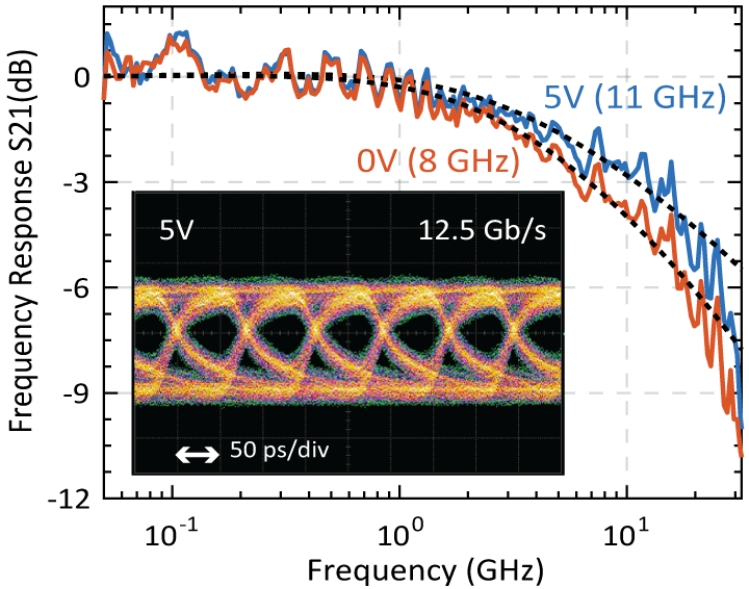


[Atabaki *et al.* Nature 2018]

Microring detectors



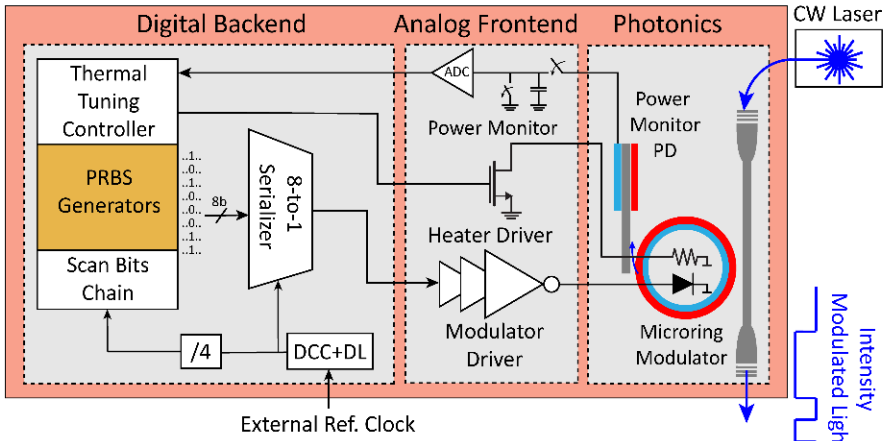


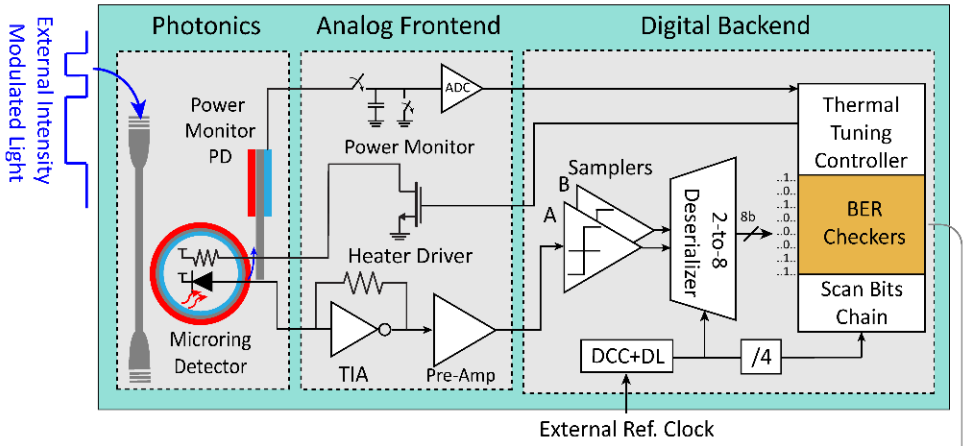


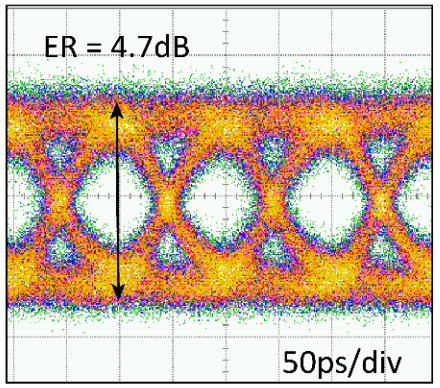
[Atabaki *et al.* Nature 2018]

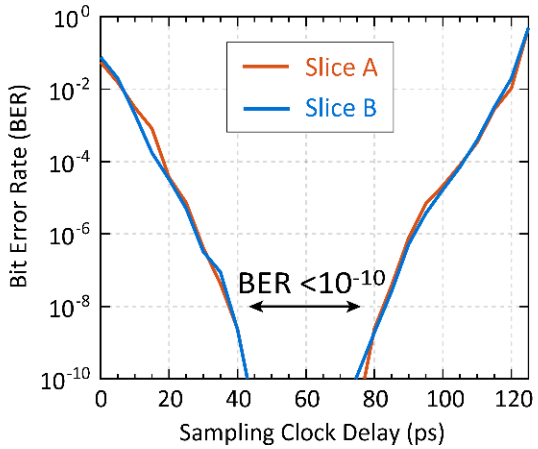
Link operation

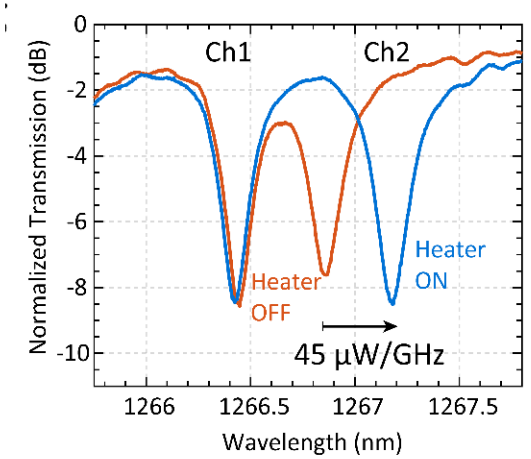
10Gbps Tx and Rx Macro Operation







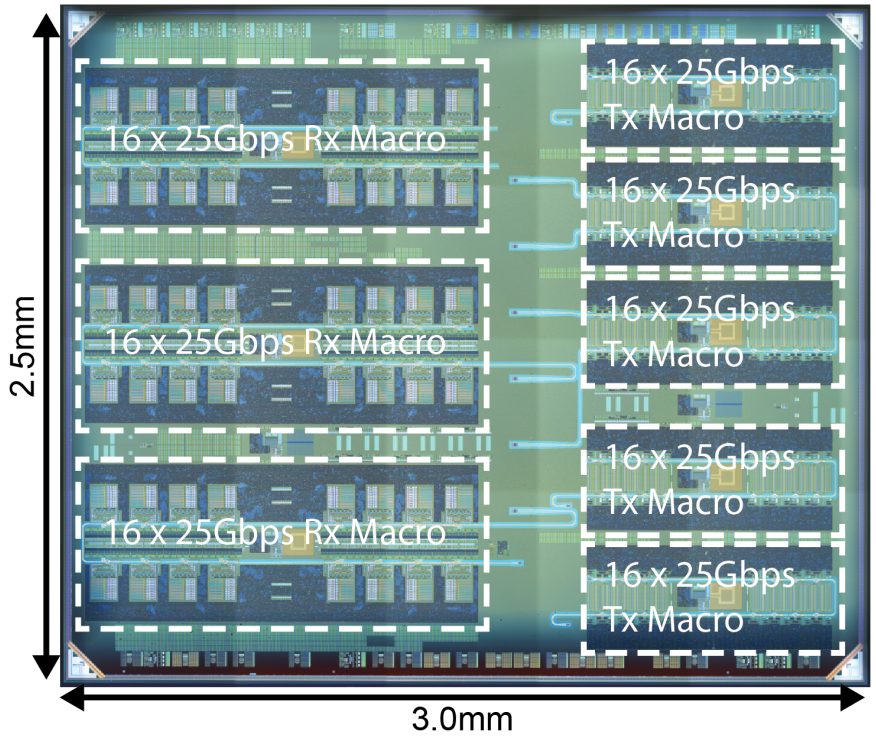


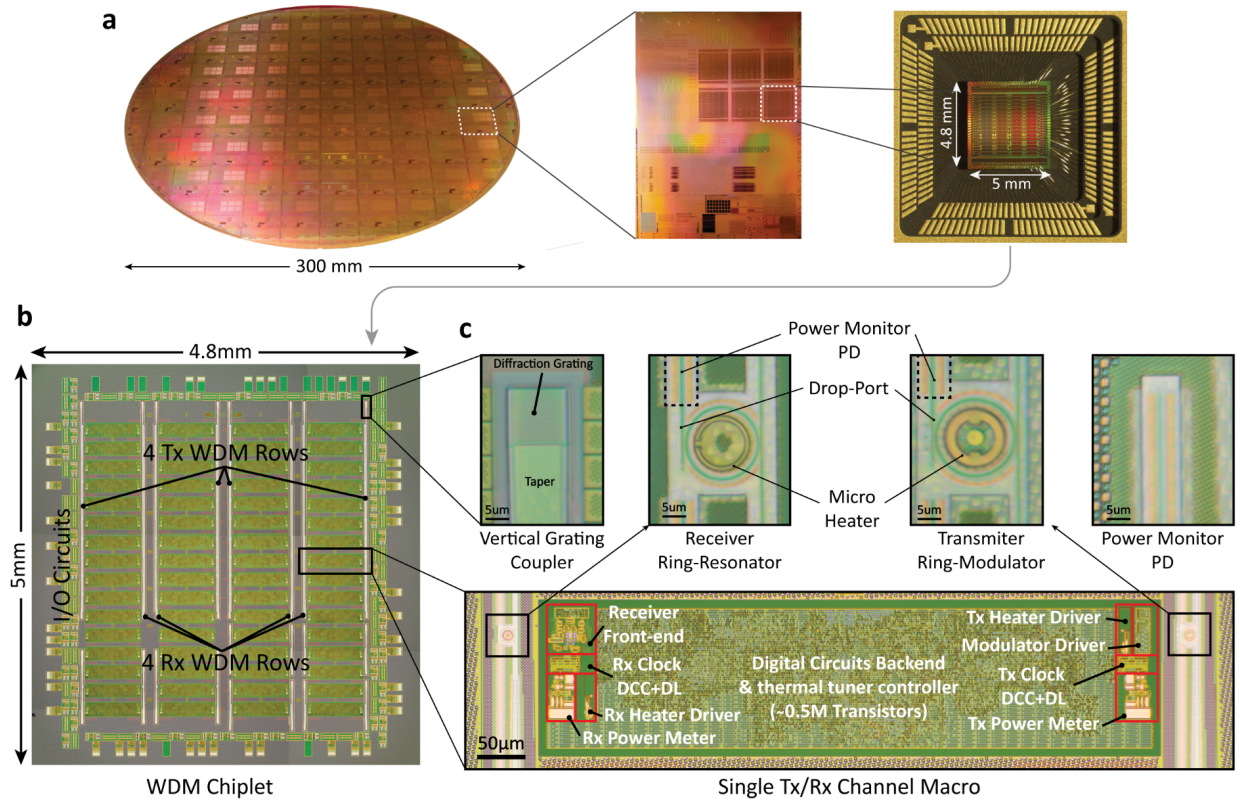


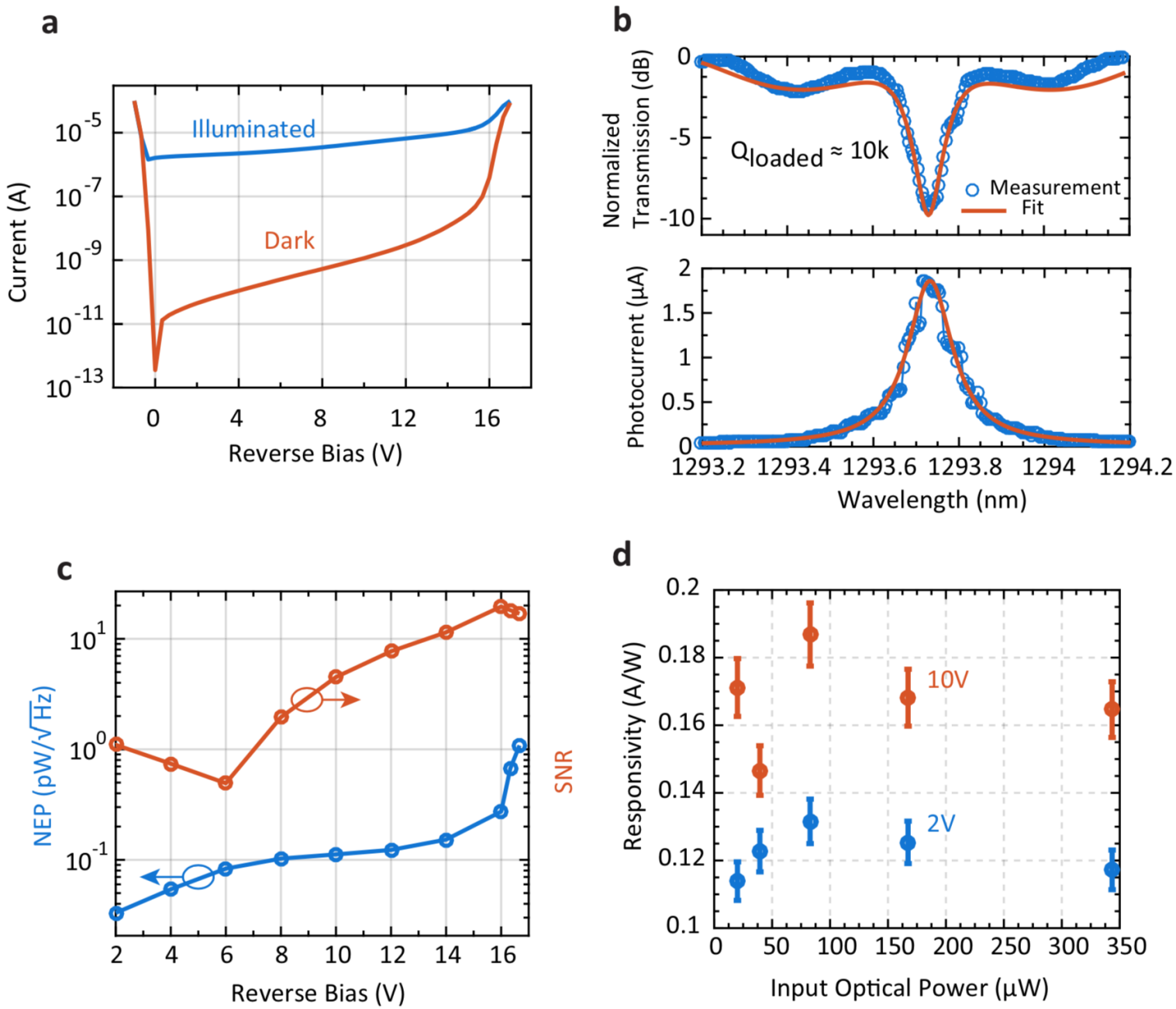
[Atabaki *et al.* Nature 2018]

Conclusions

- Photonics has entered standard CMOS processes
- An emerging ecosystem will drive new applications

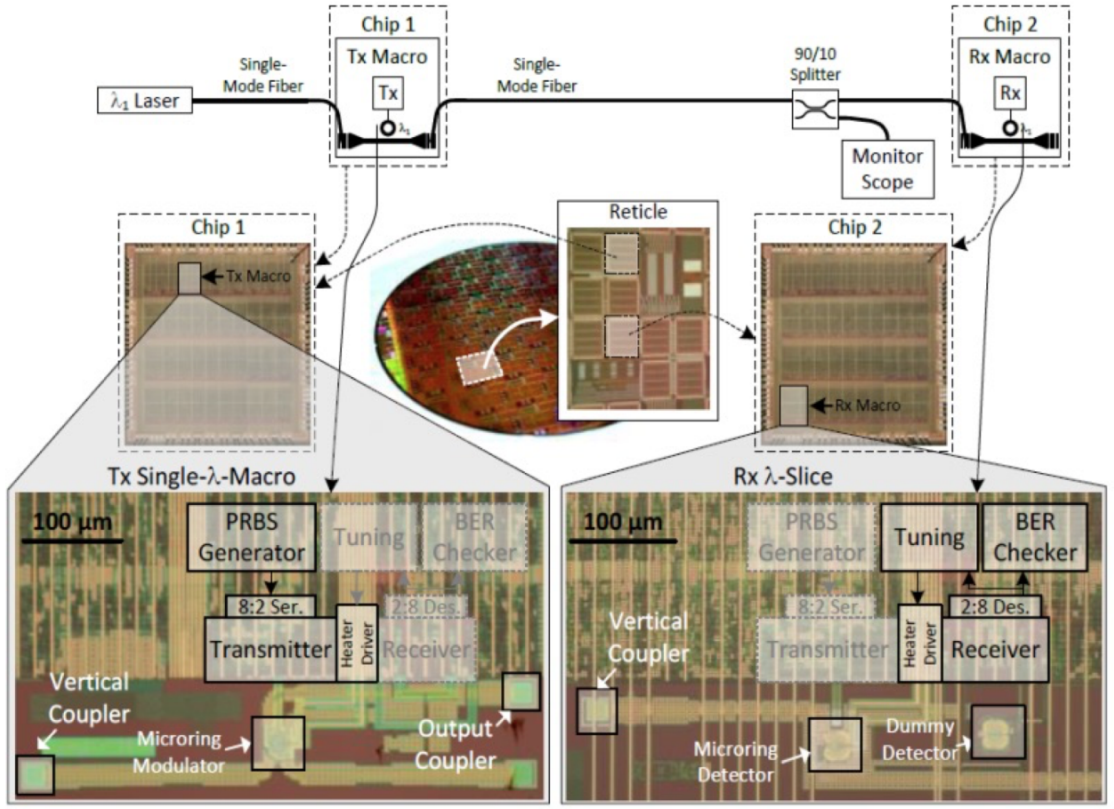




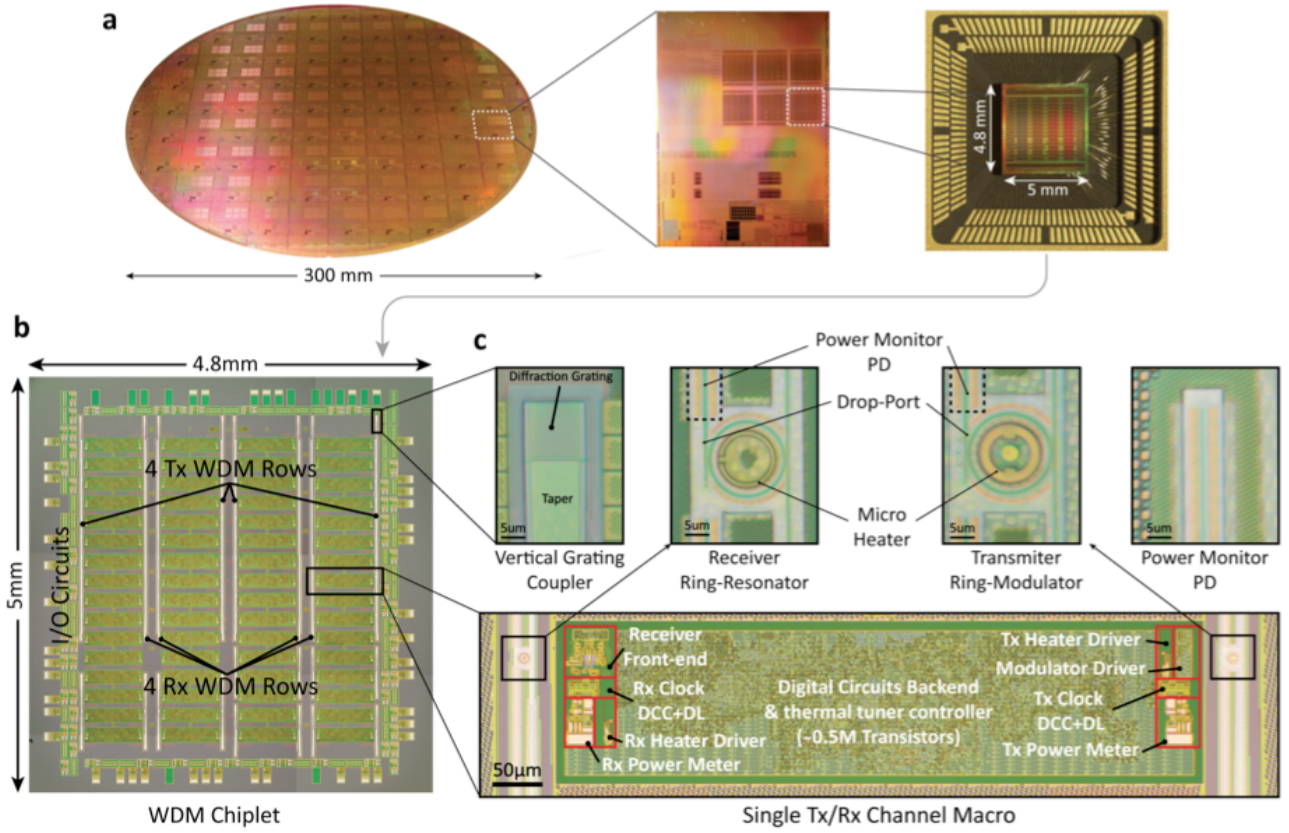


Building optics in bulk CMOS

200mm CMOS 200nm Bulk Process



300mm CMOS 65nm Bulk Process



Published this week in Nature: 65nm Bulk CMOS Integration

Integration of thin-film photonics with silicon nanoelectronics for next generation systems-on-a-chip

Amir H. Atabaki[1*†], Sajjad Moazeni[2†], Fabio Pavanello[3†¶], Hayk Gevorgyan[4], Jelena Notaros[3††], Luca Alloatti[1‖], Mark T. Wade[3**], Chen Sun[2**], Seth A. Kruger[5], Huaiyu Meng[1], Kenaish Al Qubaisi[4], Imbert Wang[4], Bohan Zhang[4], Anatol Khilo[4], Christopher V. Baiocco[5], Miloš A. Popović[4], Vladimir M. Stojanović[2] & Rajeev J. Ram[1],